Medium-term Management Plan Progress and New Financial Model

May 29, 2018

Toshiki Kawai
Representative Director, President & CEO

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- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Exchange risk
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FPD: Flat panel display

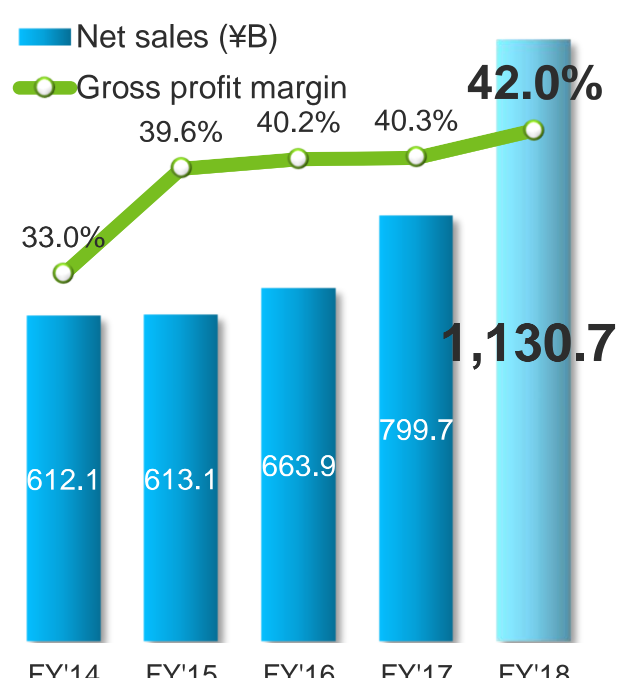
Today's Key Messages

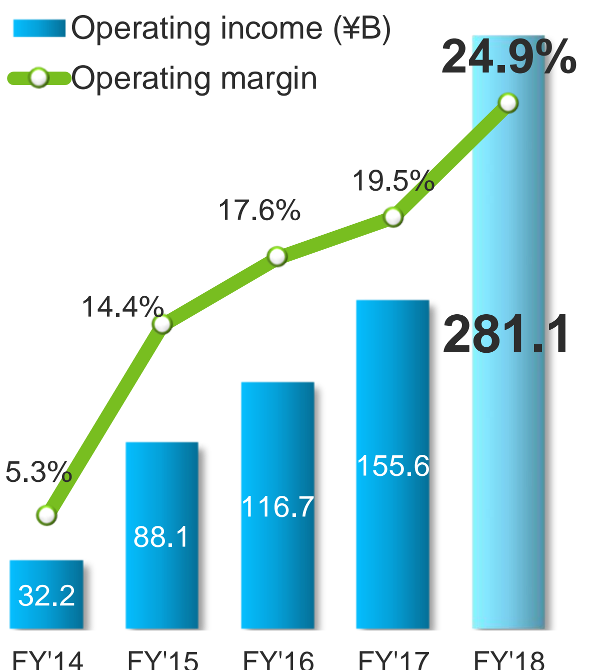
- Semiconductor production equipment market will continue to grow
  Approaching $60B+ phase

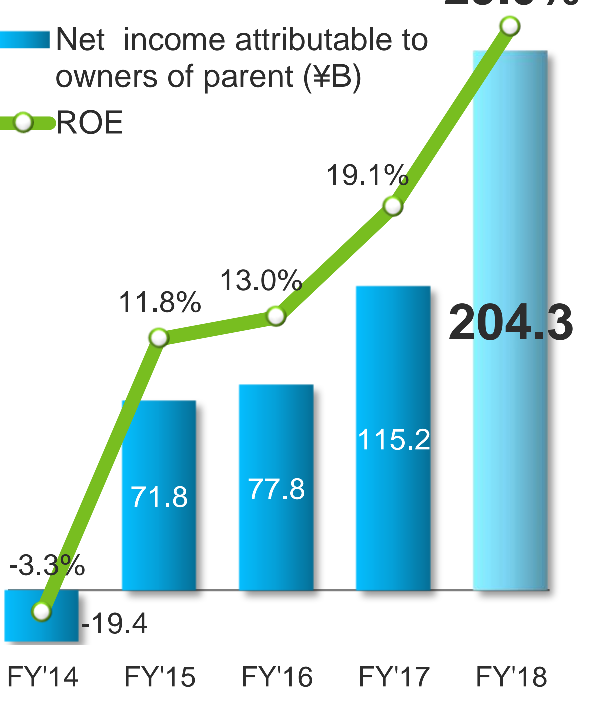
- Making good progress in business development in focus areas
  Outperform market growth

- Establish new financial model towards further growth
  Aim for world class ROE and 30%+ operating margin in the medium- to long-term

FY2018 (April 2017-March 2018) Highlights







- Net sales +41% YoY driven by the growth of the SPE* and FPD** market and expansion of market share in focus areas
- Operating income and net income attributable to owners of parent reached new record highs

* SPE: Semiconductor production equipment
** FPD: Flat panel display

FY2019 Financial Estimates

(Billion yen)

	FY2018 (Actual)	FY2019 (Estimates)			
		H1	H2	Full year	Full year YoY change
Net sales	1,130.7	690.0	710.0	1,400.0	+23.8%
SPE	1,055.2	634.0	654.0	1,288.0	+22.1%
FPD	75.0	56.0	56.0	112.0	+49.2%
Gross profit	475.0	288.0	310.0	598.0	+122.9
Gross profit margin	42.0%	41.7%	43.7%	42.7%	+0.7pts
SG&A expenses	193.8	115.0	117.0	232.0	+38.1
Operating income	281.1	173.0	193.0	366.0	+84.8
Operating margin	24.9%	25.1%	27.2%	26.1%	+1.2pts
Income before income taxes	275.2	173.0	193.0	366.0	+90.7
Net income attributable to owners of parent	204.3	128.0	142.0	270.0	+65.6
Net income per share (Yen)	1,245.48	779.95	-	1,645.20	+399.72

Expect to generate record high profits* for third consecutive year

* Net income attributable to owners of parent

Substantially Outperform Market Growth

- FY'18 results (compared to FY'17)

  ⇒ TEL sales growth **+41.4%** (WFE* market growth** **+37%**)
  Operating income growth **+80.6%**

- FY'19 estimate (compared to FY'18)

  ⇒ TEL sales growth **+23.8%** (WFE market growth **+15%**)
  Operating income growth **+30.2%**

Grow share in focus areas (etch, cleaning, ALD systems)

* WFE (Wafer fab equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.
** WFE market growth rates are for the calendar year.

Medium-term Management Plan Progress

WFE* Market size	FY'16 (Actual) $31B	FY'17 (Actual) $37B	FY'18 (Actual) $51B	FY'19 (Estimate) $58B	FY'20 financial model $42B	$45B
Net sales	¥663.9B	¥799.7B	¥1,130.7B	¥1,400.0B	¥1,050.0B	¥1,200.0B
Operating margin	17.6%	19.5%	24.9%	26.1%	24%	26%
ROE	13.0%	19.1%	29.0%	-	20-25%	

Proceed according to plan in both strengthening competitiveness of products and raising profitability

* WFE (Wafer fab equipment): The semiconductor production process is divided into front-end production, in which circuits are formed on wafers and inspected, and back-end production, in which wafers are cut into chips, assembled and inspected again. Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.
FY2016 (CY2015) market size does not include equipment for wafer-level packaging.

We Are Now at a Turning Point

Computer centric

Mobile centric

Data centric

World IP traffic

We are here

1970 1980 1990 2000 2010 2020 2030

With the spread of IoT technology the age of big data is beginning

Applications/services That Big Data Will Realize

Telemedicine

Smart cities

Smart grids

Smart mobility

IoT 5G CLOUD AI

VR/AR/MR

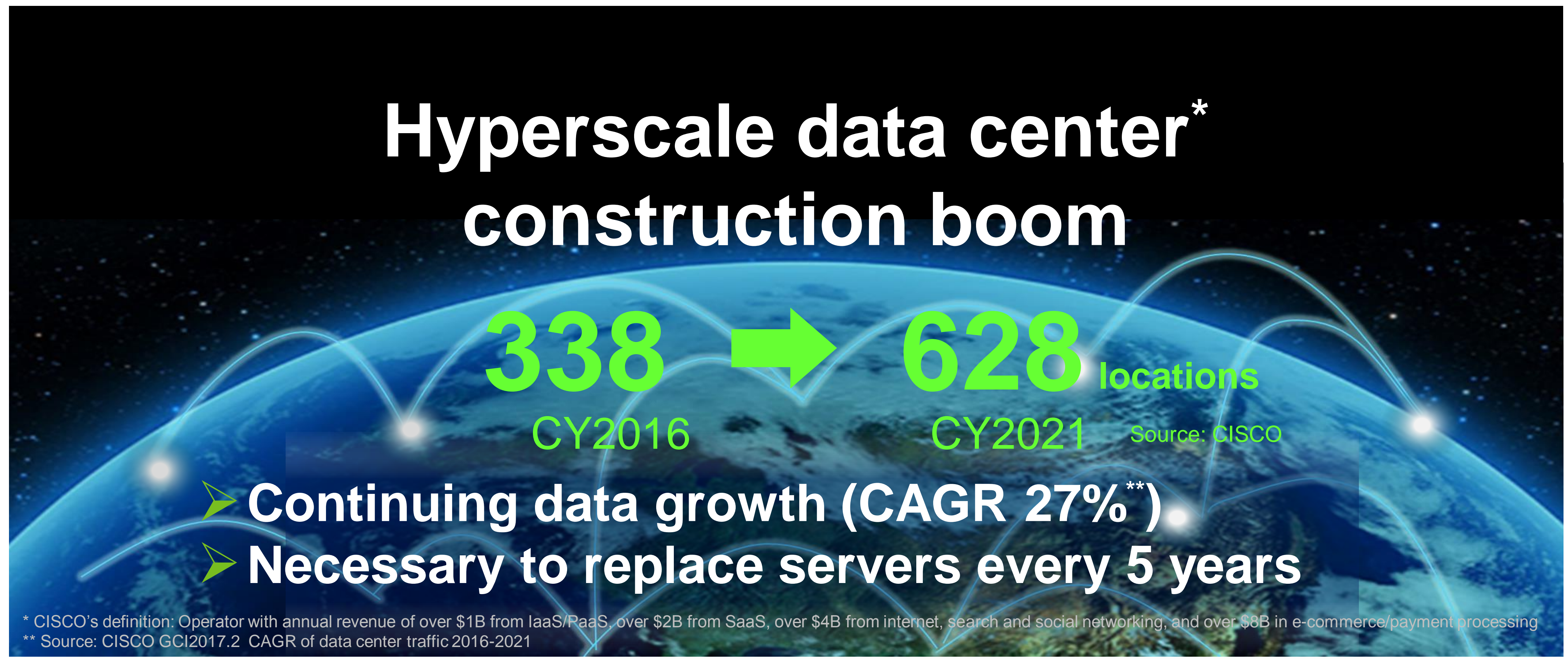
Autonomous driving

Smart fabs

Industrial robots

Demand for further technological evolution of semiconductors

Big Investment in the Cloud



Continued strong demand for memory

New Trend: Edge Computing

Cloud computing

- **Too much data to process quickly**
- **Delay: Several hundred milliseconds**

Edge computing

- **Processes data in real-time from nearby**
- **Delay: Several milliseconds**

Health platforms

Autonomous driving

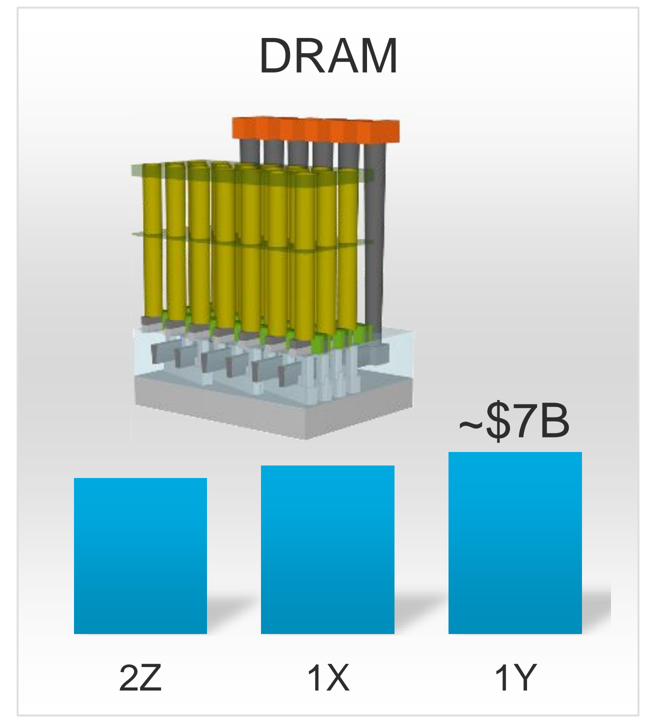
Smart fabs

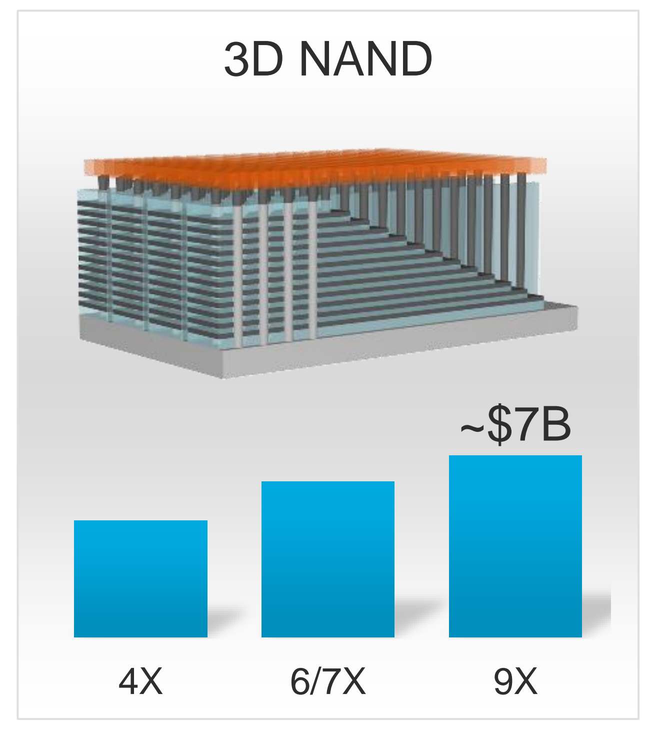
Market growth for services where delay is unacceptable

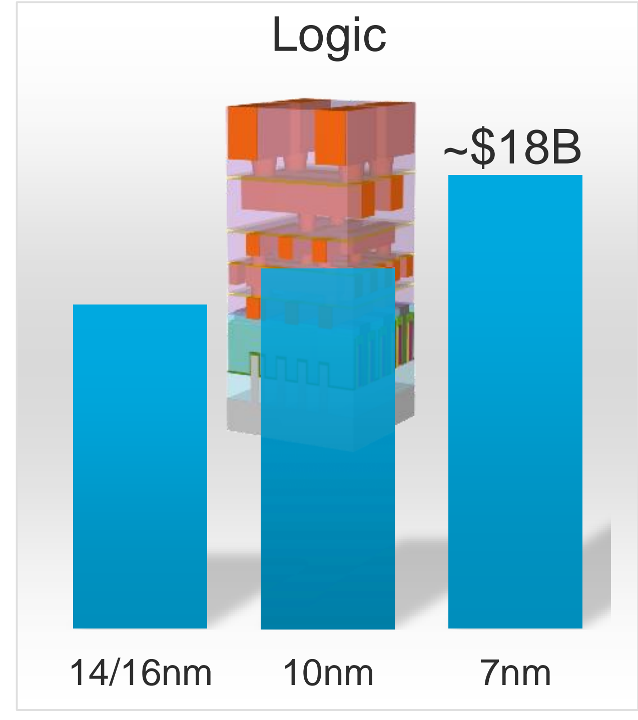
Leading-edge chips with high speed and low power consumption are essential

Rising Added-value in SPE

WFE investment (100k WSPM*, greenfield/TEL estimate)







Expanded business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

 * WSPM: Wafer starts per month

Higher Sophistication of Display Technologies

Increasing screen size

OLED

Color filter
LCD
TFT
Backlight

Emissive layer
TFT

LCD → OLED

Increasing resolution

TV: FHD → 4K → 8K

Mobile, VR: 300 ppi → 1000 ppi

Design flexibility

Flexible, edge bent, free format

Expanded business opportunities due to technological change

WFE Market Outlook

WFE market by application*

$37B
$51B
$58B
$61B
$62B
$63B

CY'16
CY'17
CY'18*
CY'19*
CY'20*
CY'21*

WLP
DRAM
Non-volatile memory
Logic foundry
Logic & others (MPU, AP, others)

* TEL estimate

WFE market approaching $60B+ phase

New Financial Model (FY2021)

WFE Market size	$55B	$62B
Net sales	¥1,500.0B	¥1,700.0B
Operating margin	26.5%	28%
ROE	30-35%	

Aim for a world class operating margin of 30%+
in the medium- to long-term

Rationale for Revisions to Financial Model

- Business development in focus areas is making good progress, and achievement of the financial model announced in May 2017 is in sight
- Over the past year it has become widely recognized that the semiconductor industry has entered a new growth stage on the expansion of new applications that support social infrastructure such as AI and IoT
- On outlook for further growth in the semiconductor industry we have upwardly revised our expected WFE market size to $62B in FY2021
- Even if WFE should shrink to $55B due to temporary market shifts, we will aspire to a management structure that is able to flexibly respond to market shifts and to secure net sales of ¥1,500.0B and an operating margin of 26.5%

Establish new financial model based on further market growth and opportunities for significant growth for TEL

Three Focus Areas for New Growth Opportunities

Make steady progress in Best Fit in New Market = "responding to diversity" and achieve Best in Class, as stated in our 2015 medium-term

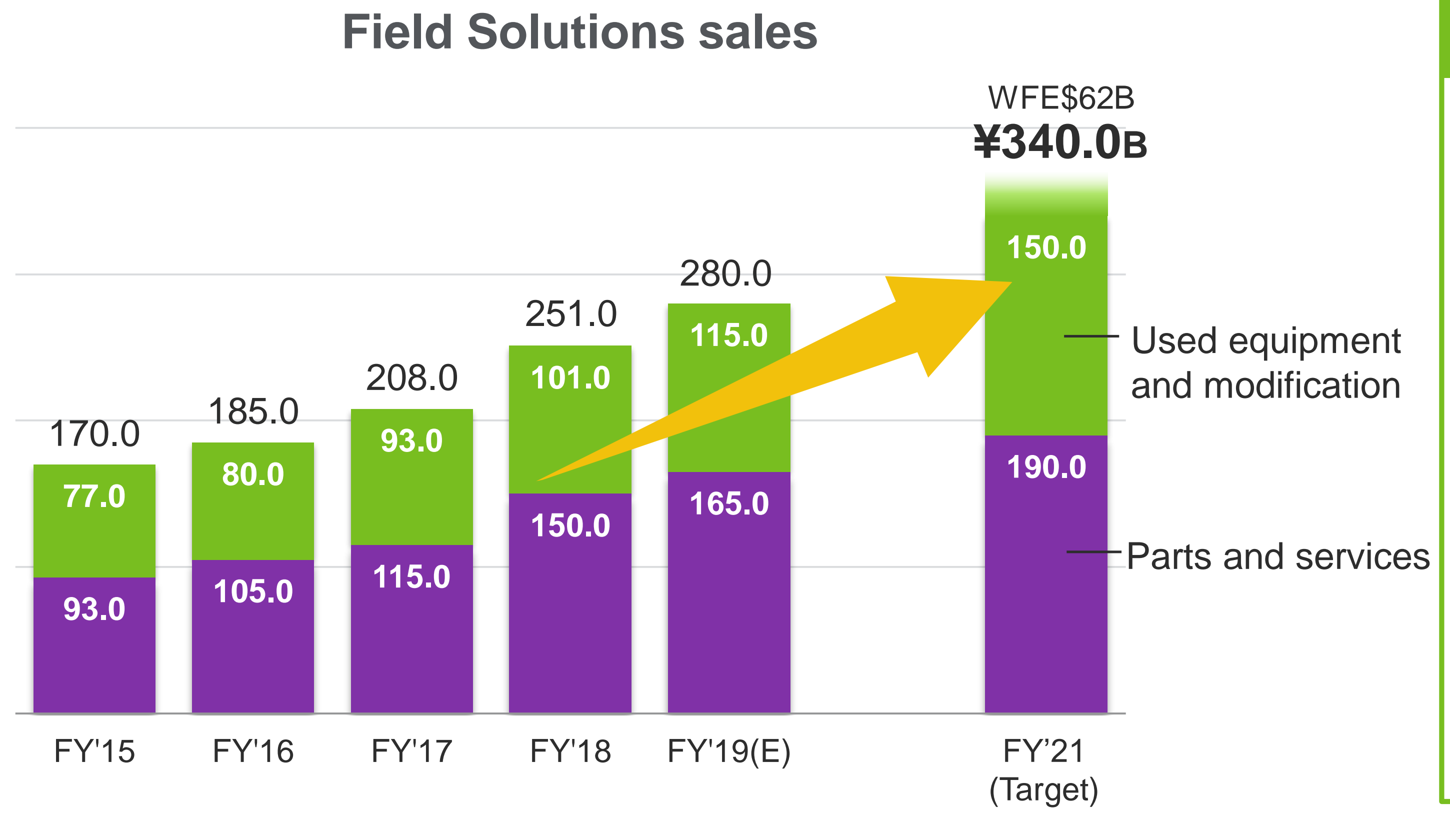
Highlights from the Past 3 Years (Initiatives to Date)

1. **Reorganization of Development & Production Group**
   - Established Process Integration Center (PIC)
   - Merged Yamanashi and Tohoku plants, established TEL Technology Solutions
   - Built new development building for etch systems (Scheduled for completion Sep. 2018)
   - Made systems intelligent through utilization of AI and IT
2. **Established new account structure (Global Field Div.)**
3. **Reorganized business units (CTSPSBU, TFFBU)**
4. **Responded to increased production (etch, deposition and test systems)**
5. **Introduced new global HR systems**

Further Promotion of Our 3 Focus Areas (Future Initiatives)

1. **Promote development of technologies that leverage TEL's comprehensive strengths**
   - Process integration technology that unites diverse technologies
   - Develop next generation platforms
2. **Promote early stage joint development and evaluation with customers**
   - Share roadmap for multi-generational technologies: shift collaboration "from dots to lines"
   - Expand onsite evaluation activity
3. **Increase productivity and added-value using data and AI**
4. **Respond to growing China business**
5. **Increase earnings in field solutions business**
6. **Promote efficiency though launch of business reform project**
7. **Implement medium-term incentive plan**

Field Solutions (FS)



Business strategy

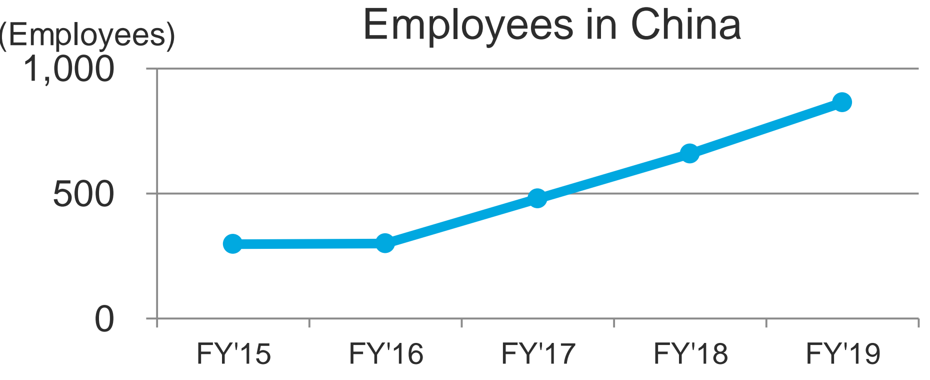
- Respond to new customer needs driven by IoT
  - Provide upgrades and remanufactured equipment that handle new applications
- Contribute to improving customer productivity
  - Provide added-value services using remote connections

(Installed base of 66,000 units)

Leverage our strengths as an equipment manufacturer to increase earnings in both the used equipment/modification and part/service segments

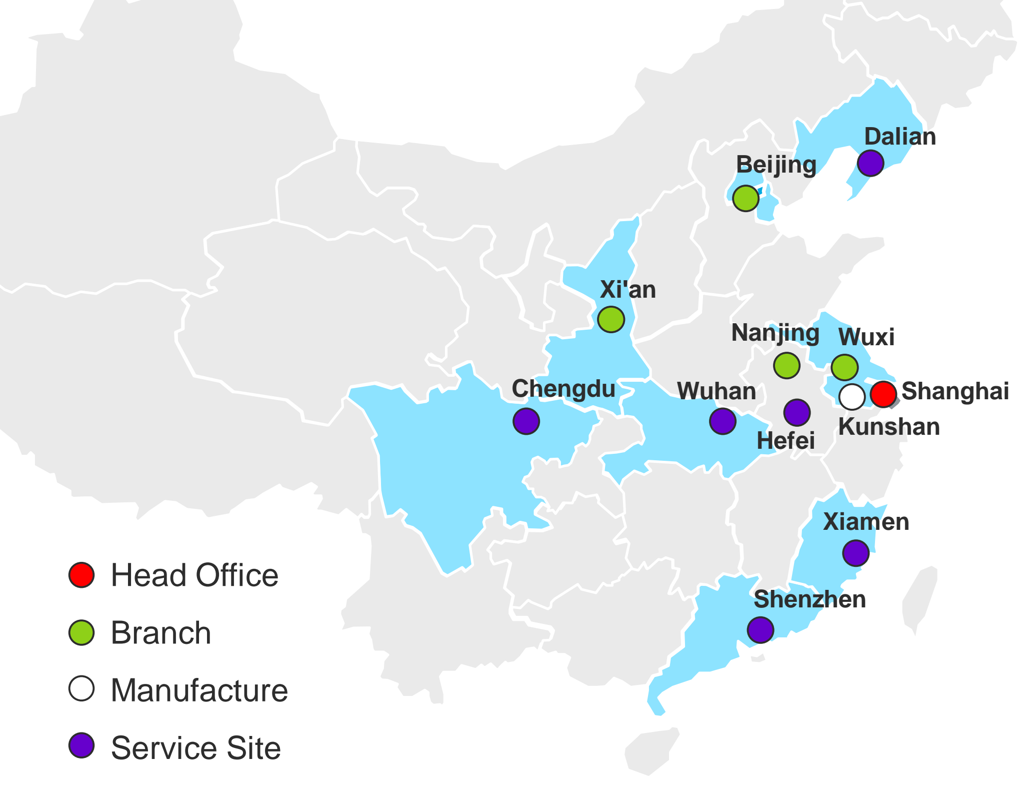
Response to Growth in China Business

- Expect China to comprise 30% of WFE (CY’20)
  - Customers planning 10-15 new plants (CY’18-CY’20)
- Capture high share and service business through high value added products and comprehensive support
- Build solid business base
  - Hiring of engineers going well (3x vs CY’16)
  - Enhance training centers



Business development in China

Opened Shanghai Office in 1998



Steadily build business base in growing market

Increasing Development and Production Capabilities

- Miyagi plant (etch systems)
  - Began operations at new logistics building, plan to raise productivity through automation
  - New development building (plan to complete by September)
  - Double production capability (plan to begin operations from October)
- Yamanashi and Tohoku plants (deposition, gas chemical etch, test systems)
  - Decided to build new production buildings
  - Strengthen BCP* with high earthquake resistance

  * BCP: Business continuity plan

Miyagi plant

Yamanashi plant: approx. ¥13.0B construction cost (Begin construction in January 2019, completion scheduled for April 2020)

Tohoku plant: approx. ¥13.0B construction cost (Begin construction in October 2018, completion scheduled for September 2019)

Secure development and production capabilities in line with further growth stage

TEL's Sustainability (economic value × social value = corporate value creation)

- Going forward, continue to work to resolve social issues and contribute to the achievement of sustainable development goals (SDGs) through our business activities in accordance with the Ten Principles of the UN Global Compact and RBA* code of conduct

Environment	Climate change, water, biodiversity, environmental management
Social	Human rights, employment and labor, health and safety, supply chain, local communities
Governance	Corporate governance, compliance, risk management

MEMBER OF
Dow Jones Sustainability Indices
In Collaboration with RobecoSAM

Continue to be a company trusted by all stakeholders

* RBA: Responsible business alliance

Contributing to the Environment is a Key Strategy

Lower energy consumption of TEL products + **Manufactured devices realize low power consumption**

Raises TEL's value

Technological proposals that reduce environmental impact create significant value

New Financial Model (FY2021)

(Billion yen)

WFE market Market share	FY2018 (Actual) $51B 14%	FY2019 (Estimates) $58B 15%	FY2021 (Plan) $55B 18%	FY2021 (Plan) $62B 18%
Net sales	1,130.7	1,400.0	1,500.0	1,700.0
SPE	1,055.2	1,288.0	1,400.0	1,600.0
FPD	75.0	112.0	100.0	100.0
Gross profit	475.0	598.0	650.0	745.0
Gross profit margin	42.0%	42.7%	43.3%	43.8%
SG&A expenses	193.8	232.0	252.0	269.0
SG&A expenses to sales ratio	17.1%	16.6%	16.8%	15.8%
Operating income	281.1	366.0	398.0	476.0
Operating margin	24.9%	26.1%	26.5%	28.0%
Net income attributable to owners of parent	204.3	270.0	292.0	348.0
Net profit margin	18.1%	19.3%	19.5%	20.5%

Increase corporate value through innovative technologies and groundbreaking proactive solutions, raise efficiency and secure even higher profitability and resistance to market shifts

Gross Profit, SG&A Expenses (Sales ¥1,700.0B Model)

(Billion yen)

	FY2018 (Actual)	FY2019 (Estimates)	FY2021 (Plan)	Growth rate (FY'18-FY'21)
Gross profit	475.0	598.0	745.0	+57%
Gross profit margin	42.0%	42.7%	43.8%	+1.8pts

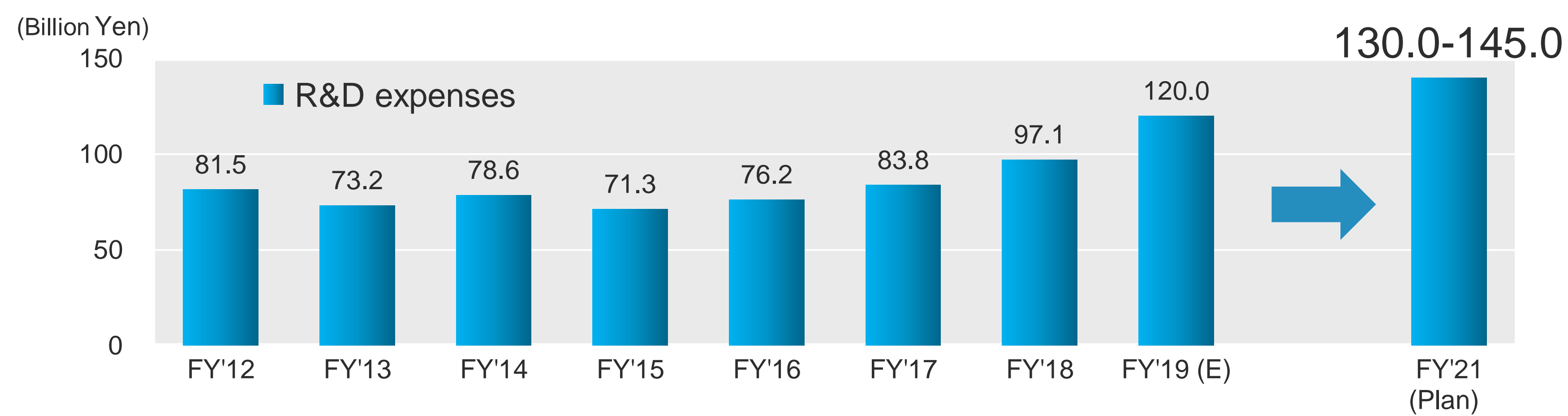
- Raise gross profit margin of core SPE, FPD products
  - Timely introduction of new products to an expanding market
  - Lower cost ratio through product quality improvements

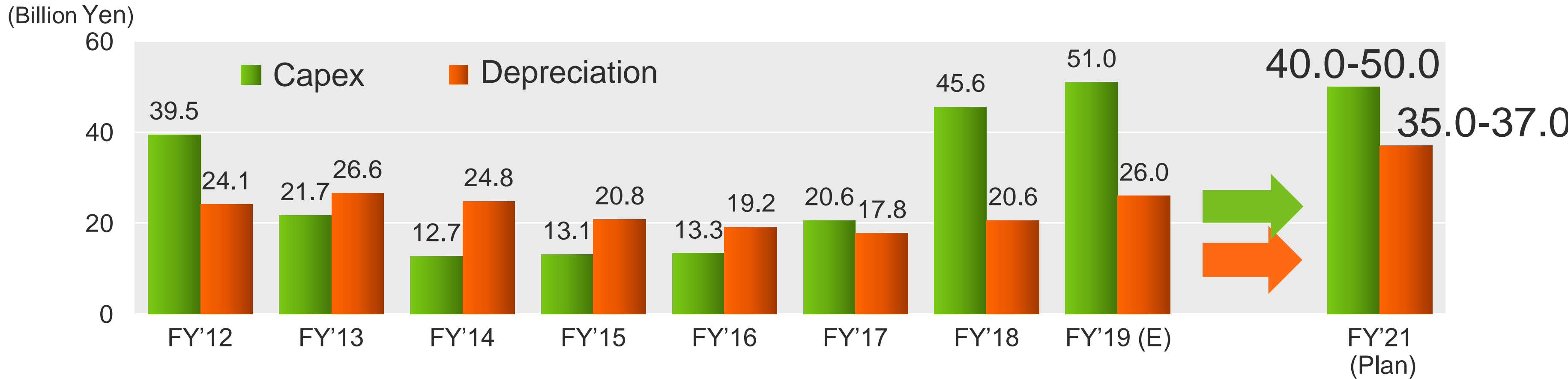
(Billion yen)

	FY2018 (Actual)	FY2019 (Estimates)	FY2021 (Plan)	Growth rate (FY'18-FY'21)
SG&A expenses	193.8	232.0	269.0	+39%
SG&A expenses to sales ratio	17.1%	16.6%	15.8%	-1.3pts

- Proactively invest in growth areas while planning appropriate SG&A and R&D expenses

R&D Expenses, Capex Plan

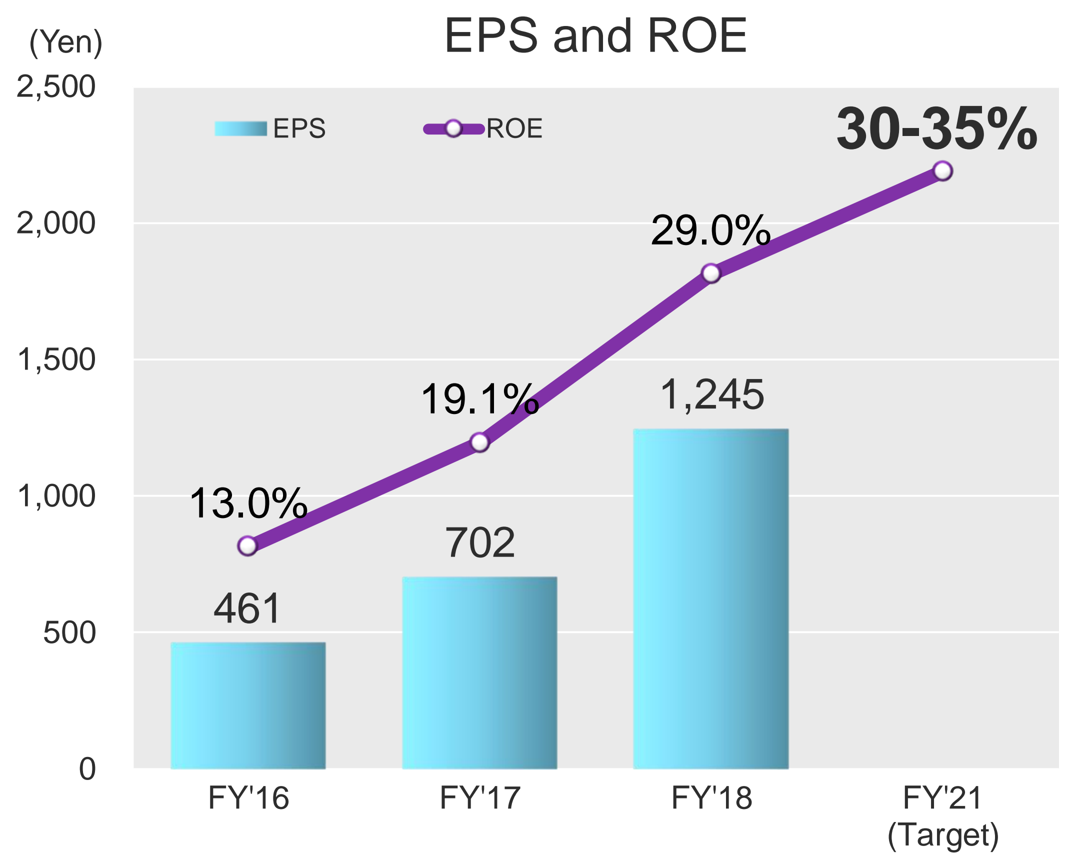




Conduct proactive investment towards further growth

Assets and Capital Efficiency (Sales ¥1,700.0B Model)

- Accounts receivable turnover
  - Current: 52 days ⇒ Achieved target
- Inventory turnover
  - Current: 111 days ⇒ Target: **95 days**
- ROE
  - Current: 29% ⇒ Target: **30-35%**



Maintain focus on assets and capital efficiency

Capital Policy, Shareholder Returns

- Approach to capital policy
  - While closely monitoring the business environment and our necessary cash balance, we will strive to raise ROE through earnings maximization and by raising capital efficiency
- Approach to shareholder return policy (basically linked to performance)

Dividend payout ratio: 50%

Annual DPS of not less than ¥150

We will review our policy if the company does not generate net income for 2 consecutive fiscal years

We will flexibly consider share buybacks

No change in shareholder return policy

Summary

- Establish new financial model backgrounded by expected growth in semiconductor and production equipment markets. Aim for short, medium and long term growth
- Aim to increase sales beyond market growth rate through stronger competitiveness of products and deeper cooperation with customers
- Raise development efficiency and business productivity and secure even higher profitability and resistance to market shifts

Aim for sustained growth in corporate value through a management base with global-standard strength

Evolving Semiconductor Device Application and the Future of Process Technology

May 29, 2018

Akihisa Sekiguchi, Ph.D.
VP & GM, Deputy General Manager, Technology Strategy Division,
Advanced Semiconductor Technology Division, Global R&D

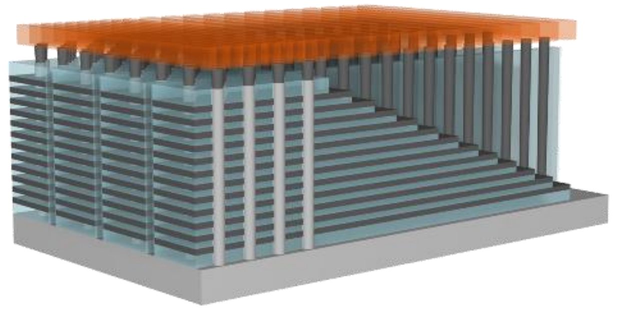
Outline

- Trends and issues in semiconductor process technology:
  Mainstream devices (CMOS Logic, NAND, DRAM)
- Technology challenges deep dive: Logic devices
- Devices that may drive further growth of the WFE market in the future
  autonomous driving enablers and AI
- Summary

Trends and Issues in Semiconductor Process Technology

Process Technology Issues for Major Semiconductor Devices

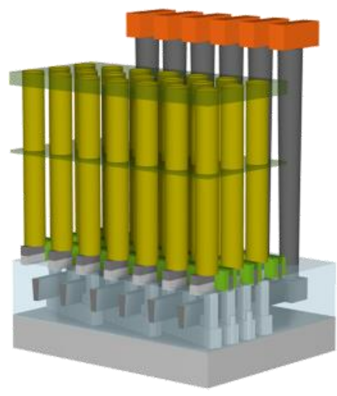
3D NAND



Multi-layering & productivity

High selectivity process
Realizing highly uniform process suitable for 3D structures

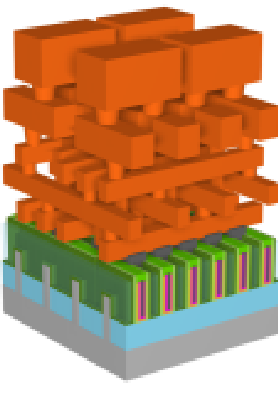
DRAM



Enhancements from 1Y-1Z

High aspect ratio process, enhanced precision and material specific adaptation to achieve higher bit density

Logic

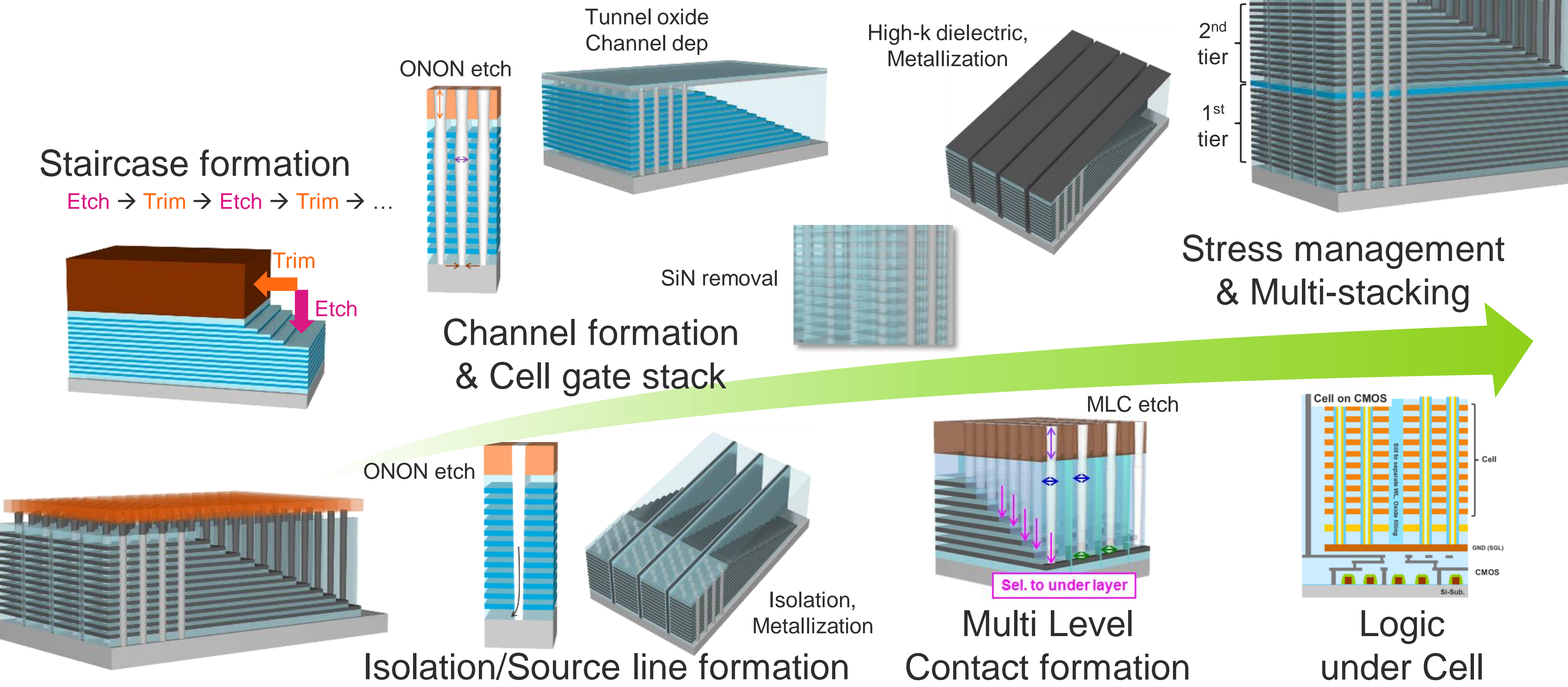


5 & 3 nm development

Precision patterning process co-optimized for device design and new materials

Drive collaboration in & out of the company to accelerate creation of innovative process technologies

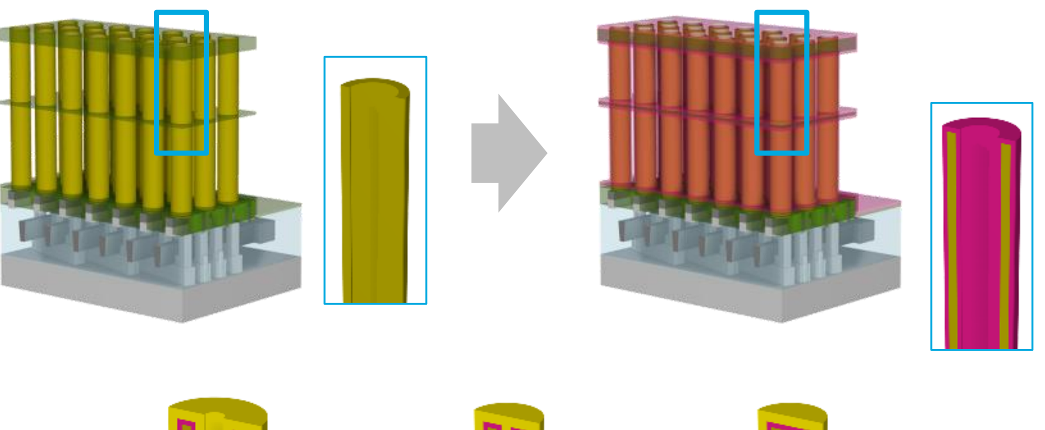
3D NAND Technical Issues

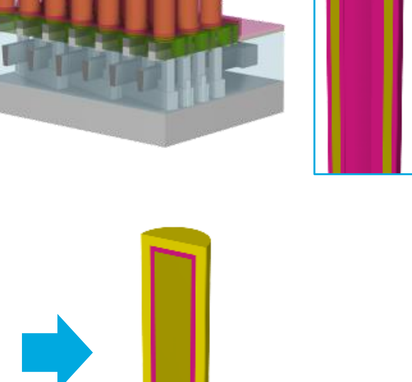


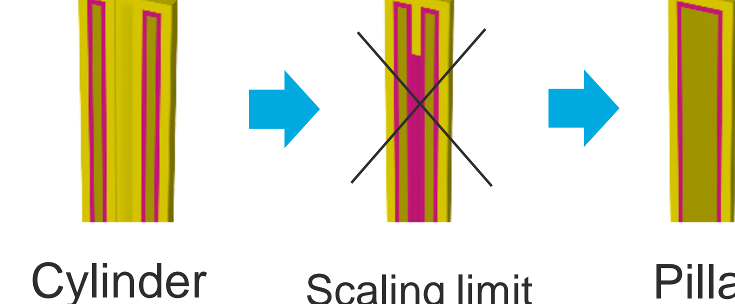
Increasing number of layers requires a variety of new technical solutions

DRAM Technical Issues

High-k dielectric deposition







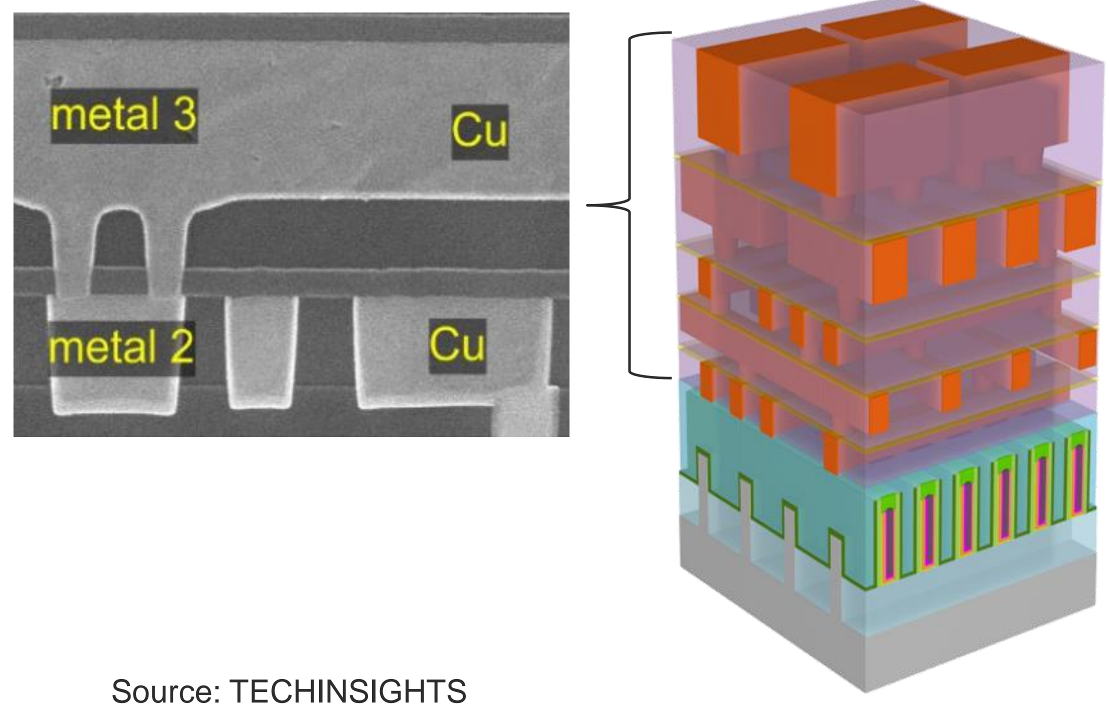
Cylinder (Present)

Scaling limit

Pillar (Future)

Needs higher-k and lower leak current

From Al to Cu wiring



Source: TECHINSIGHTS

Higher capacitance → Higher dielectric constant

RC delay due to miniaturization → Introduction of logic Cu interconnects

Technology Challenges Deep Dive: Logic Devices

Device Scaling Trends

3D Architecture

Nanowire FET

FinFET

[nm]

	1990	1993	1996	1999	2002	2005	2008	2011	2014	2017	2020

Light source: i-Line, KrF, ArF, Immersion ArF, EUV

Technology node: 130, 110, 90, 65, 45, 32, 22, 14, 10, 7, 5

Y axis: 1000, 100, 10, 1

Scaling

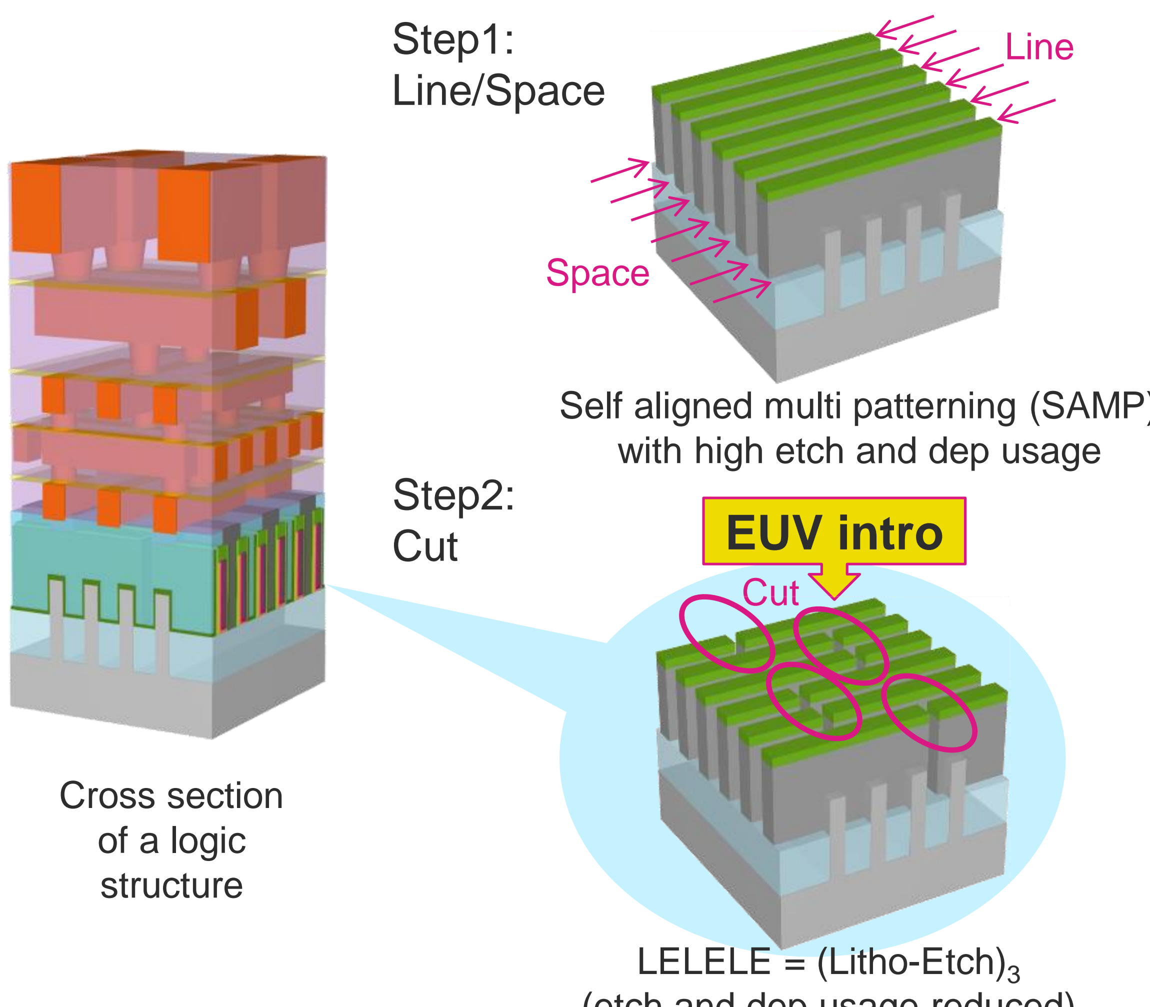
Planar FET

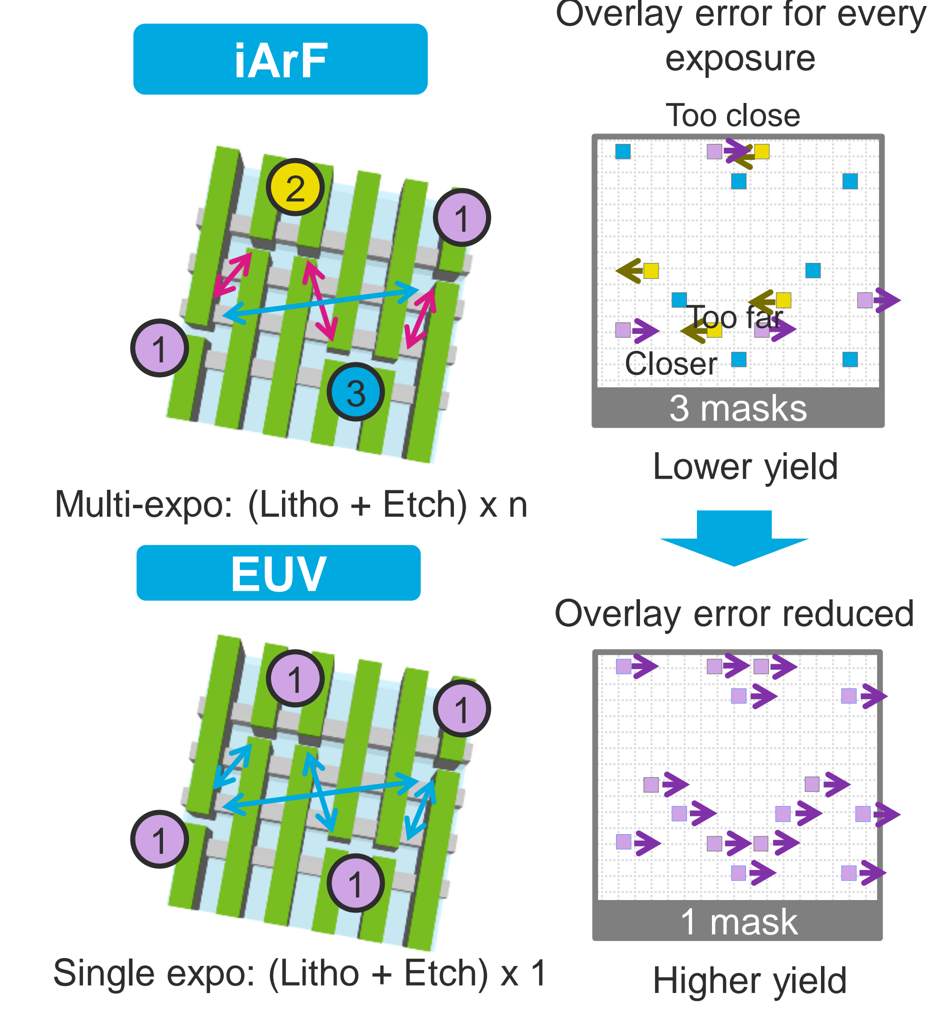
Poly gate

High-k/metal gate

Complex 3D processes to realize N3
EUV slowly gets manufacturing adoption

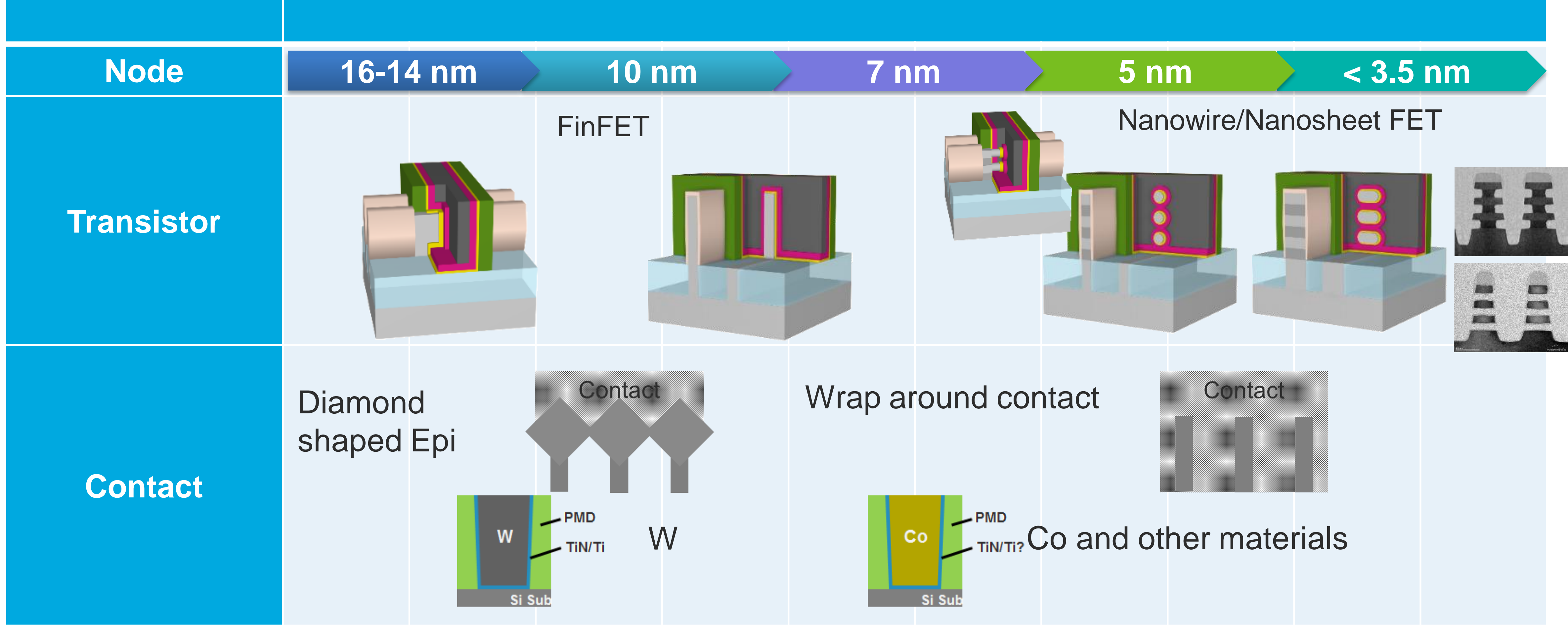
Scaling Issue: Overlay





EUV reduces overlay error but SAMP is still in use

Logic FEOL/MOL Technology Roadmap



Scaling and performance enhancement concurrently requires structure, design and material changes, which makes integration challenging

Complexity of the Fabrication Processes for Logic Devices

Nanowire FET

PolySi
HfSiON
TiN
10nm

R. Coquand et al., VLSI tech. 2013

Precise control in an atomic level

Wrap around contact (WAC)

Courtesy of imec

Self-aligned contact (SAC)

Conventional patterning

half pitch 12 12

etch

Multi-color patterning

pitch 36 36

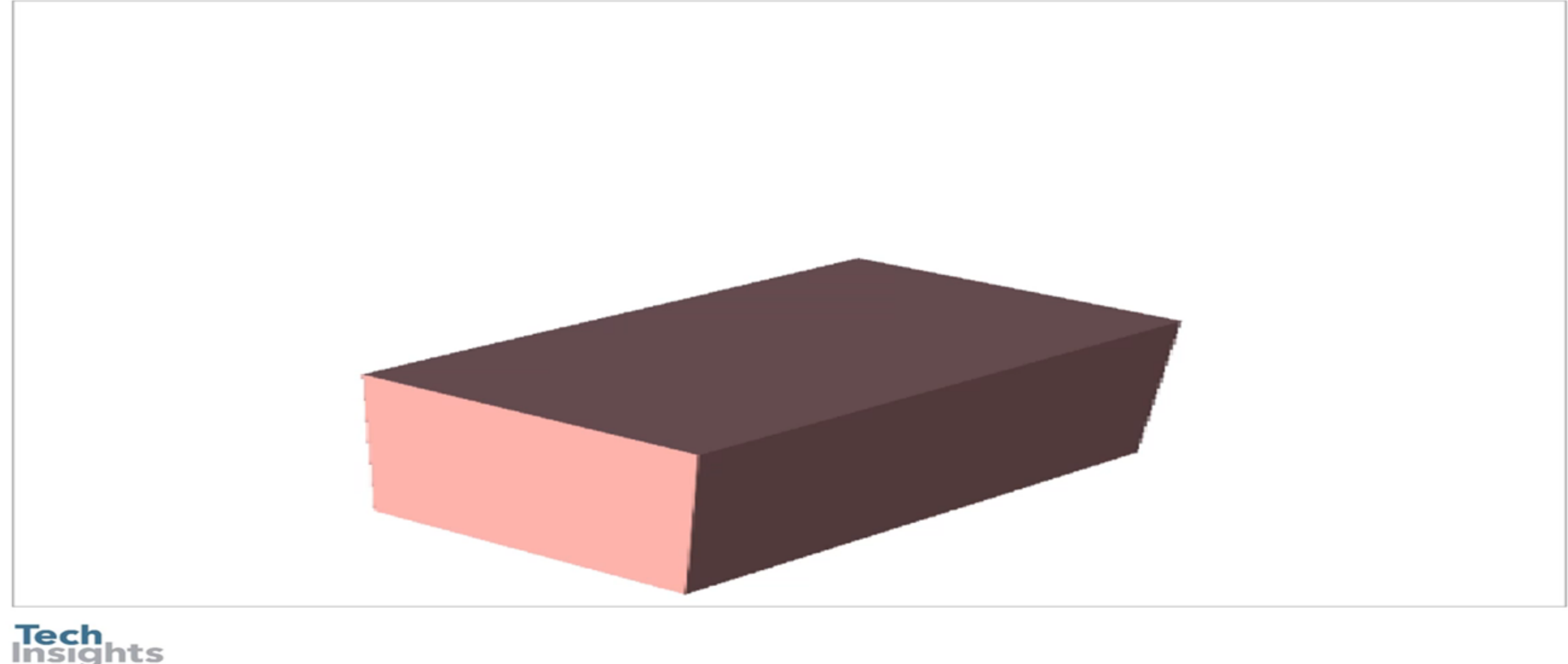
etch

Applications		N+1	N+2	N+3
FEOL	Patterning and hard mask	Known	Known	Known
	Nanowire FET			Unknown
MOL	Patterning and hard mask	Known	Known	Known
	Contact structure (WAC)		Unknown	Unknown
	New plug material (Ru)		Unknown	Unknown
BEOL	Patterning and hard mask	Known	Known	Known
	EUV productivity		Unknown	Unknown
	Selective deposition			Unknown
Common	Pitch imbalance control			Unknown

Known | Unknown

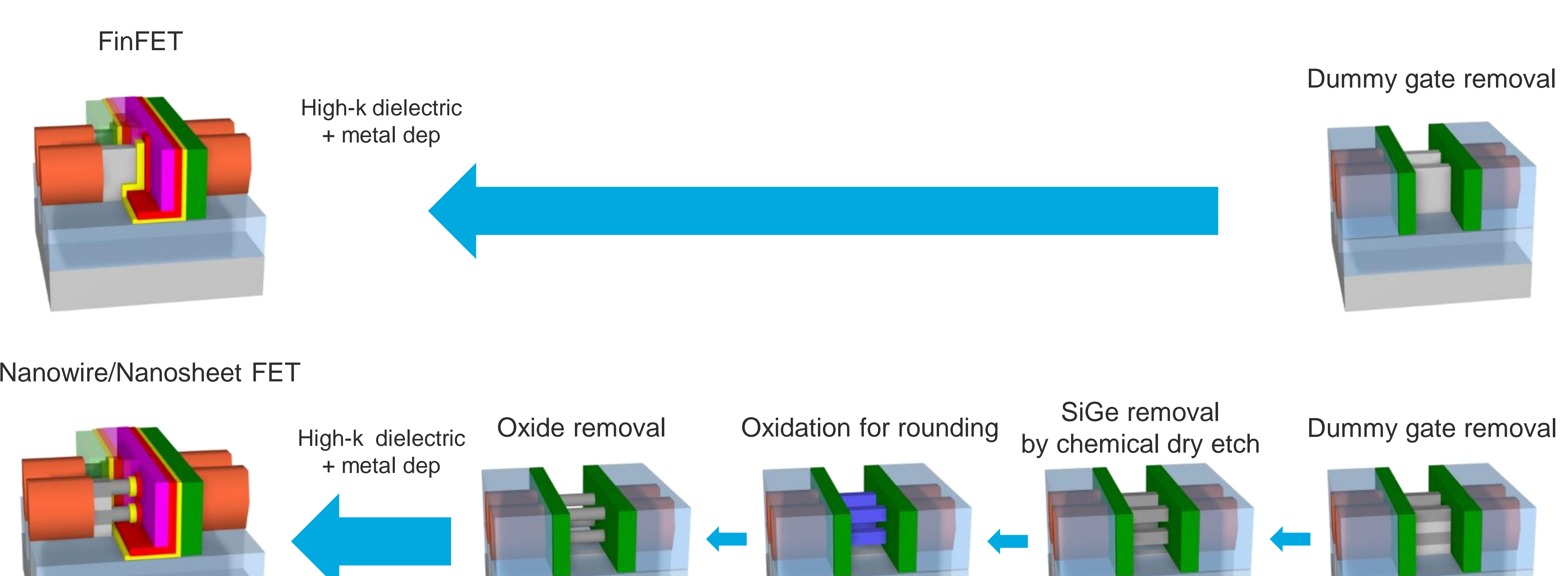
Design and process technology co-optimization is a challenging integration issue

Major Semiconductor Devices: FinFET



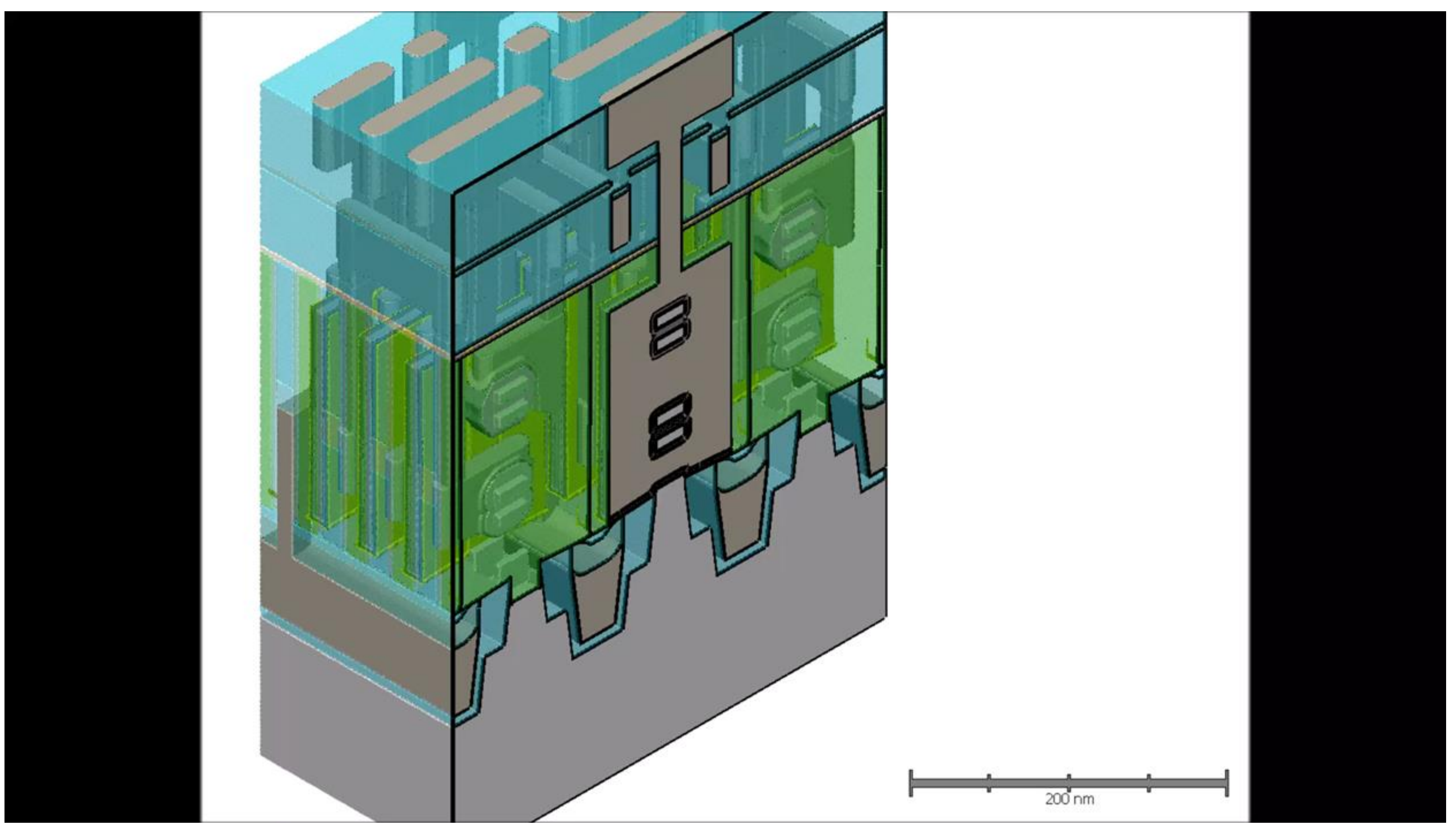
FinFET formation alone is a complicated process

Challenges in Nanowire/Nanosheet Fabrication



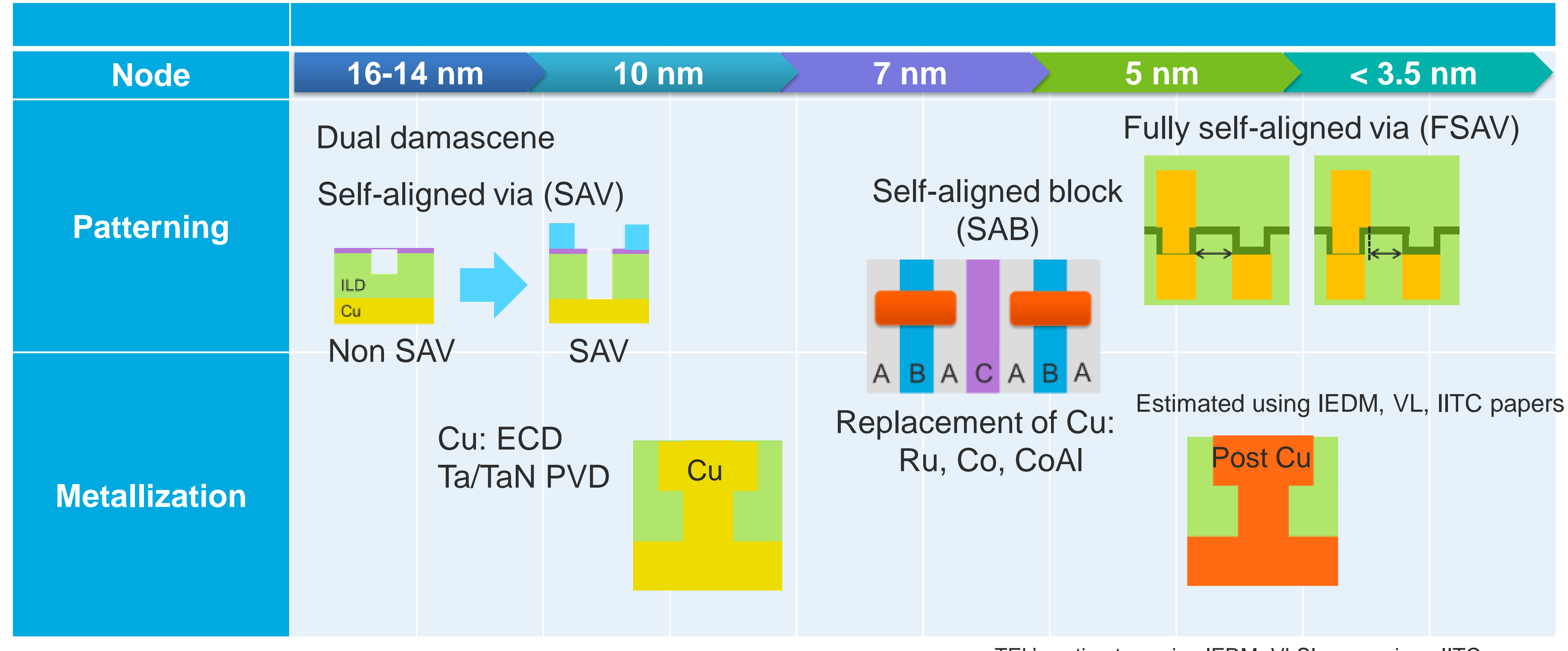
Nanowire/Nanosheet formation is even more complicated than FinFET

New Semiconductor Devices CFET



Structural formation modelling and electrical simulation are now a must

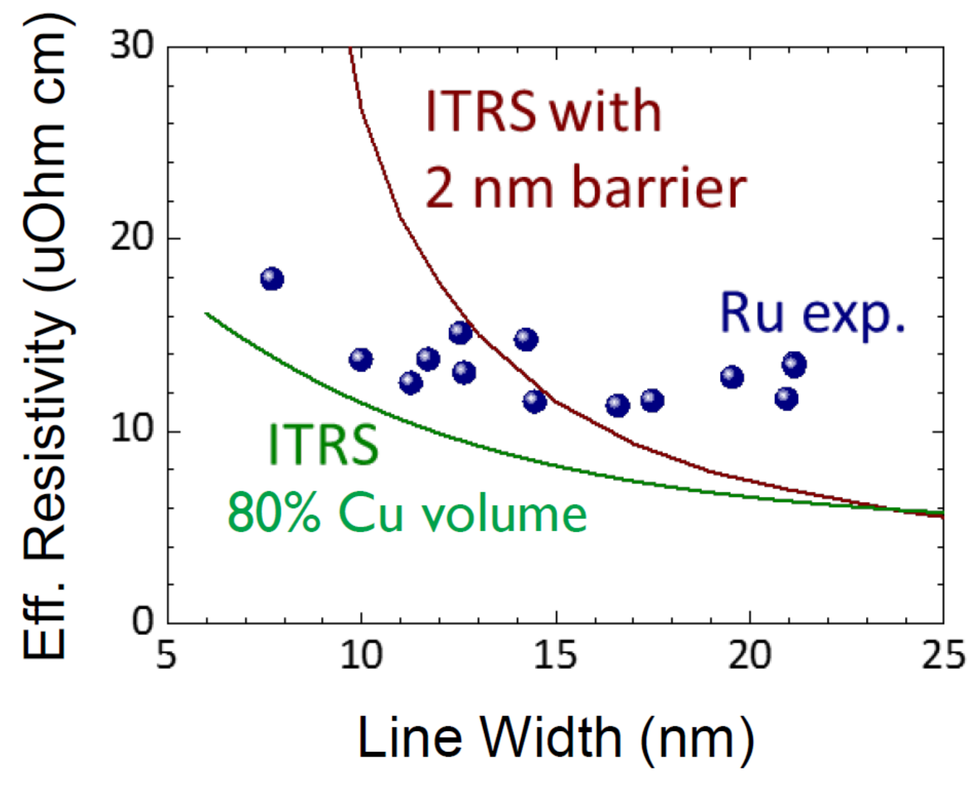
Logic BEOL Technology Roadmap



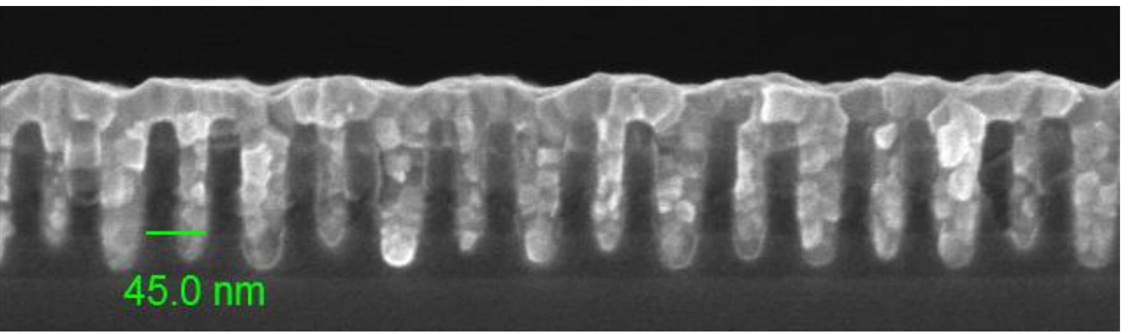
TEL's estimates using IEDM, VLSI symposium, IITC papers

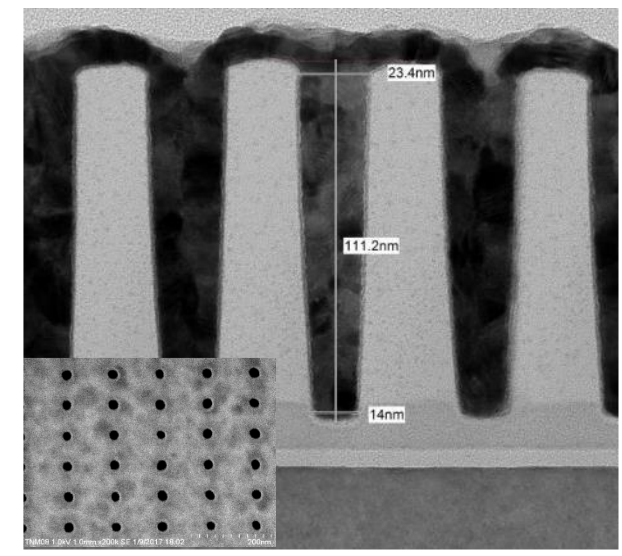
Scaling and overlay issues require new integration schemes

R&D for Future Growth: Beyond Cu



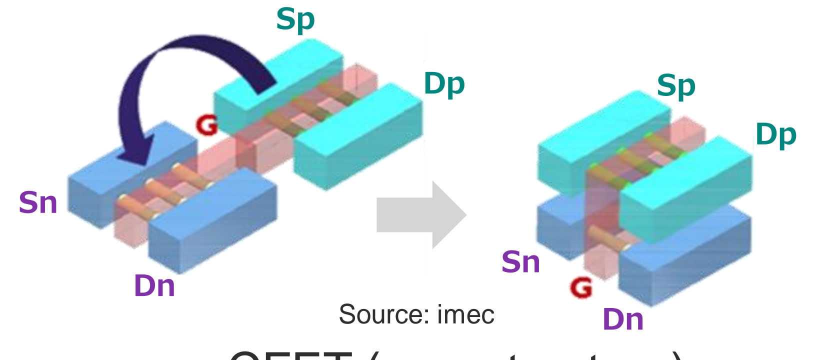
Source: An Steegen, imec technology forum 2017





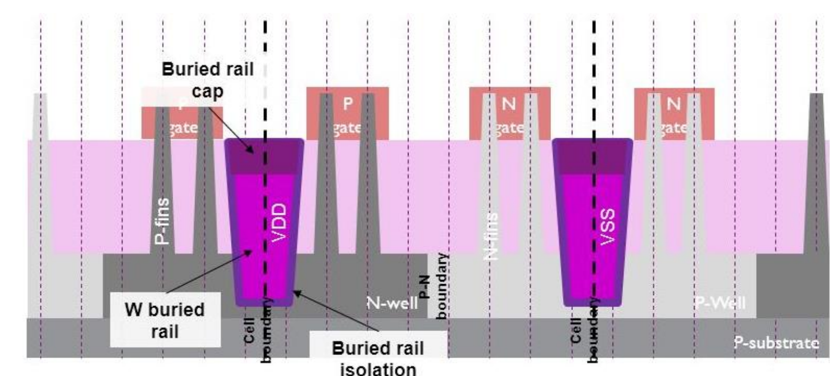
Line width reduction is pushing copper to its limits
→ New material required

New Opportunities through Integration



Source: imec

CFET (new structure)



Buried power rail (new material)

Source: Imec presentation at ISPD 2016

Tactras™ Vigus™

Etch

EXPEDIUS™-*i*

Cleaning

Certas™

CELLESTA™-*i*

Lithography

EXIM™

CLEAN TRACK™ LITHIUS Pro™ Z

TELINDY PLUS™

NT333™

Triase*e*+™

Deposition

Close integration between process equipment is a must in order to propose solutions to realize further scaling through new materials and structural solutions

TEL

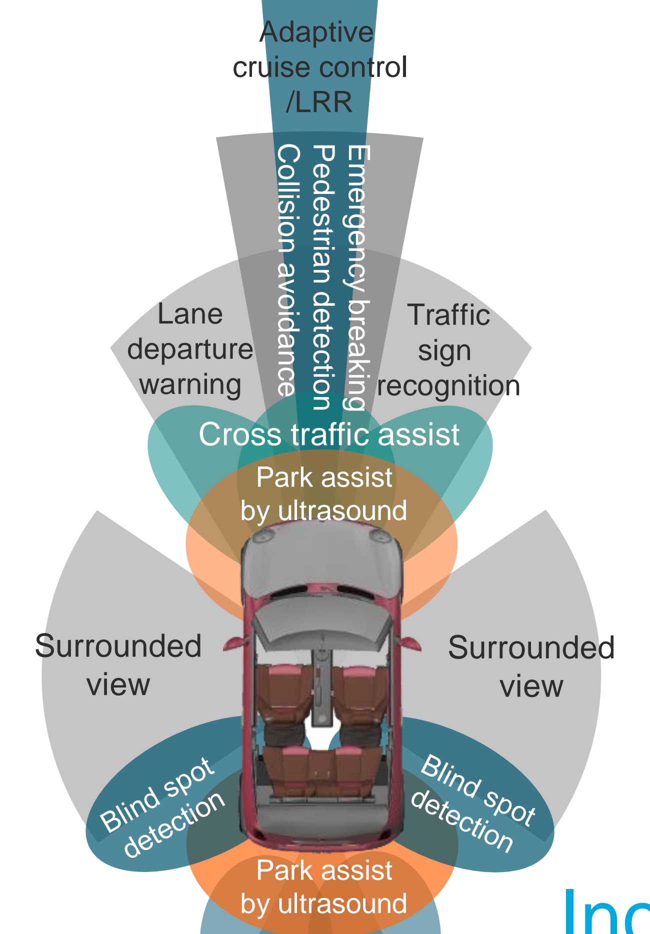
Devices That May Drive Further Growth of the WFE Market in the Future Autonomous Driving Enablers and AI

Autonomous Driving

https://blog.caranddriver.com/nhtsa-sides-with-google-officially-declares-autonomous-car-software-a-driver-sorta/

Semiconductor usage will increase
with the arrival of autonomous driving

Higher Automotive Functionality



- Hybrid vehicles use 2.5-3 times more semiconductor devices compared to conventional gasoline vehicles
- Electric vehicles use even more than 2x
- With ADAS*, additional value add is $50-$100
- Autonomous driving vehicles transit 6TB of data daily to Data Centers

- ADAS today uses 6 cameras per vehicle
- In the near future, ~10 per vehicle
  - Interior, driver, passenger monitoring
  - AR/VR
  - Airbag control

* ADAS: Advanced driver assistance system

Increase in semiconductor usage from conventional gasoline, hybrid, electrical, to autonomous vehicles (not to mentions the infotainment data related adders)

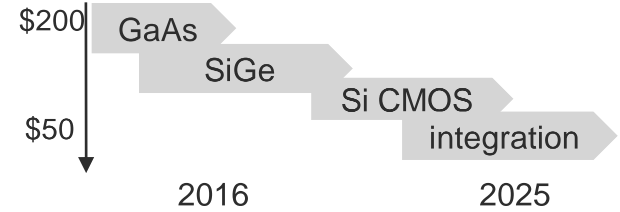
ADAS・Device Challenges for Autonomous Driving

- **Viewing, Sensing camera**
  - Front 1-2, back1-3, CIS
  - In the future 10-12
  - Higher pixel density
  - Faster image readout
  - Processing circuit

- **LiDAR* cost**

  (Infrared laser scan in 3D)
  - High end LiDAR: ~few million yen
  - Motorless MEMS version will drive cost below 50,000 yen

- **mm radar**
  - Higher resolution, wider angle
  - From SiGe to Si CMOS (~2019)
  - Integrated communication IC and micro controller (~2022)



- **Processor/Memory/ECU****
  - CPU under autonomous driving use a few KW
  - DRAM degradation under high temp (refresh cycle)
  - Using auto temperature grade LPDDR4
    - High temp tolerant DRAM cell
    - Error reduction circuit
    - Data/ECC*** transmission function
  - Flexible ECU development

* LiDAR: Laser imaging detection and ranging ** ECU: Engine control unit *** ECC: Error correction code

Semiconductor Use Increase Due to Autonomous Driving

Mid-end board for autonomous driving

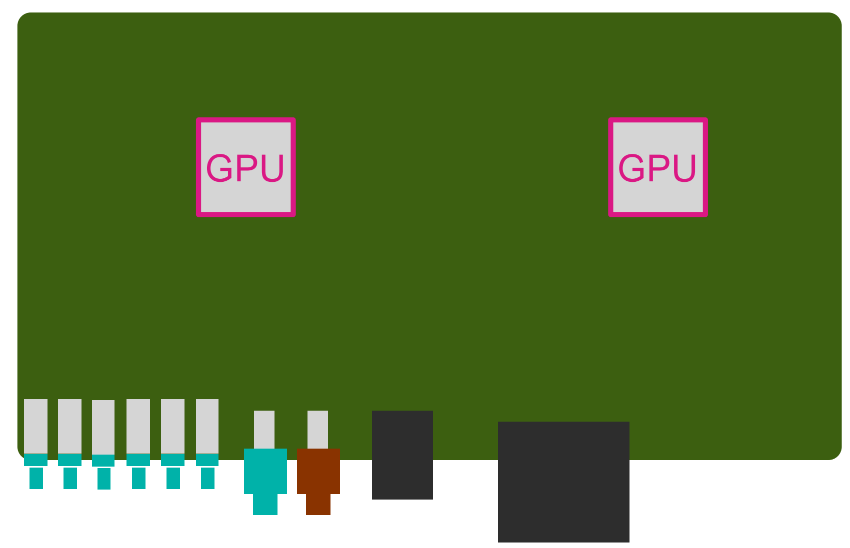
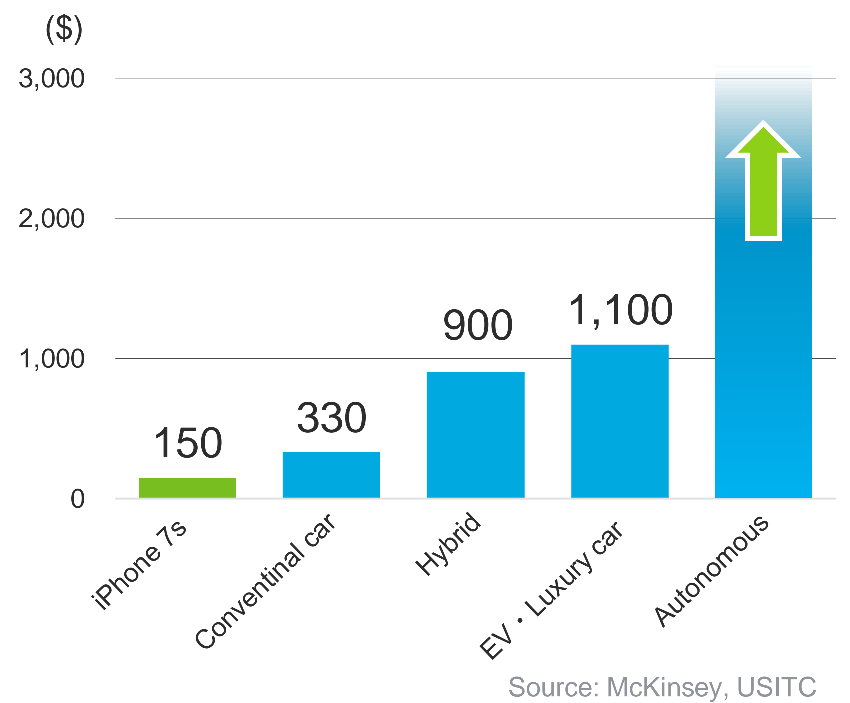


Image of GPU size relative to the board

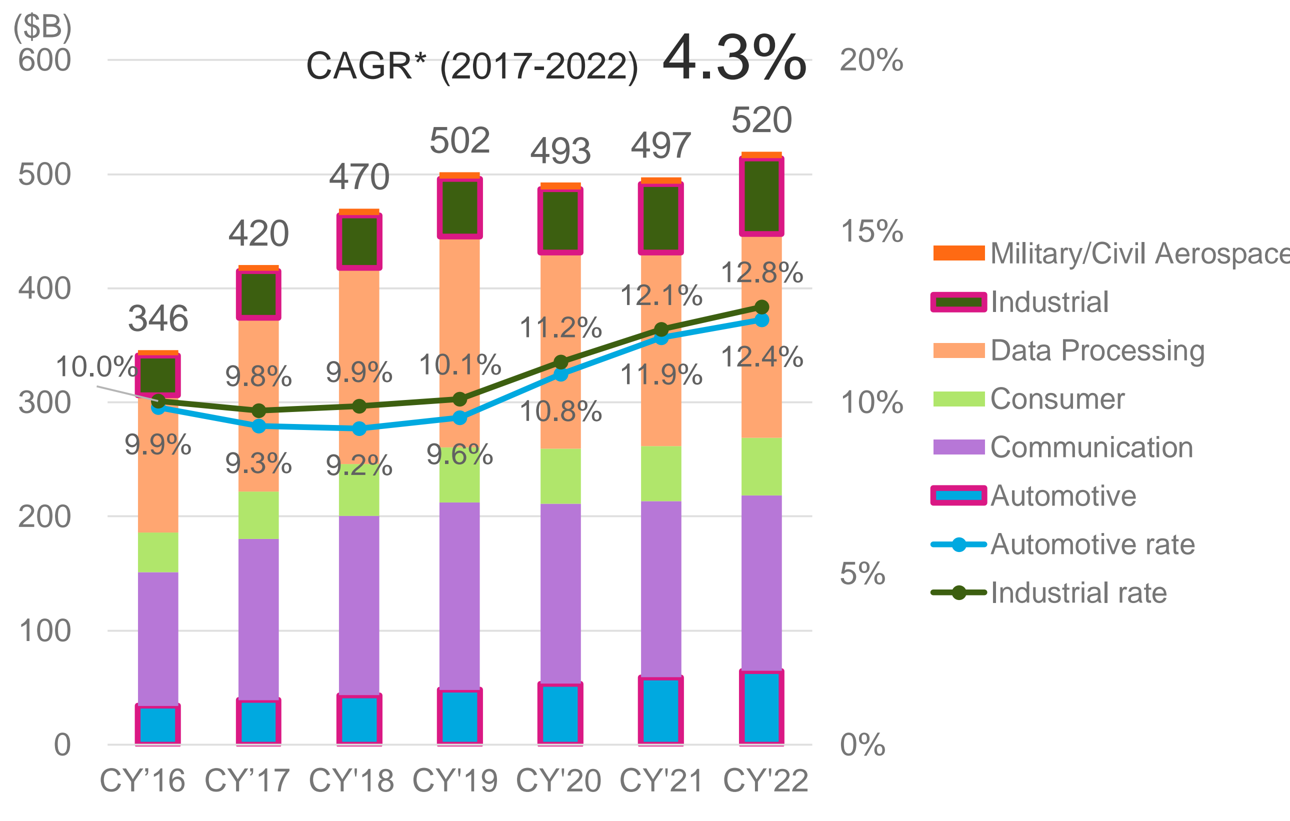
Semiconductor usage per vehicle



Source: McKinsey, USITC

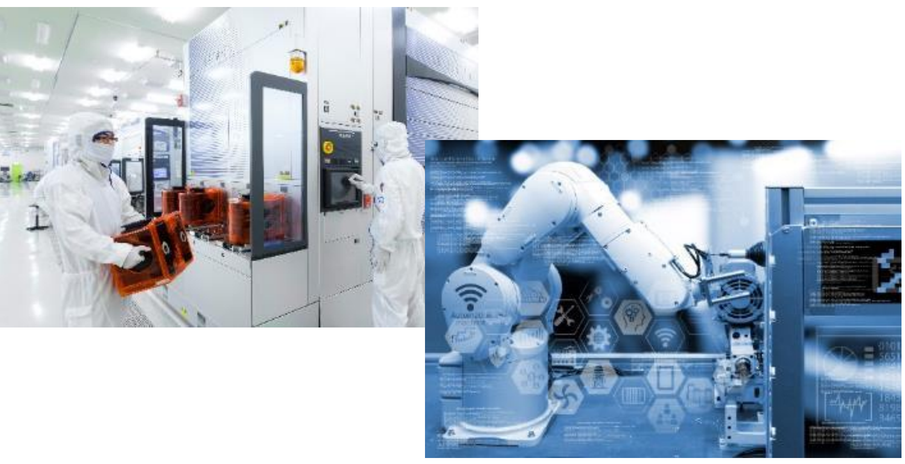
Autonomous driving vehicles may use 10x (cost) in terms of semiconductors versus conventional gasoline vehicles

Semiconductor Sales Amount



Source (Worldwide Semiconductor Forecast): Gartner, "Semiconductor Forecast Database, Worldwide, 1Q18 Update", 3 April 2018,
Charts/graphics created by Tokyo Electron based on Gartner research

Industrial app semiconductor CAGR 10.1%

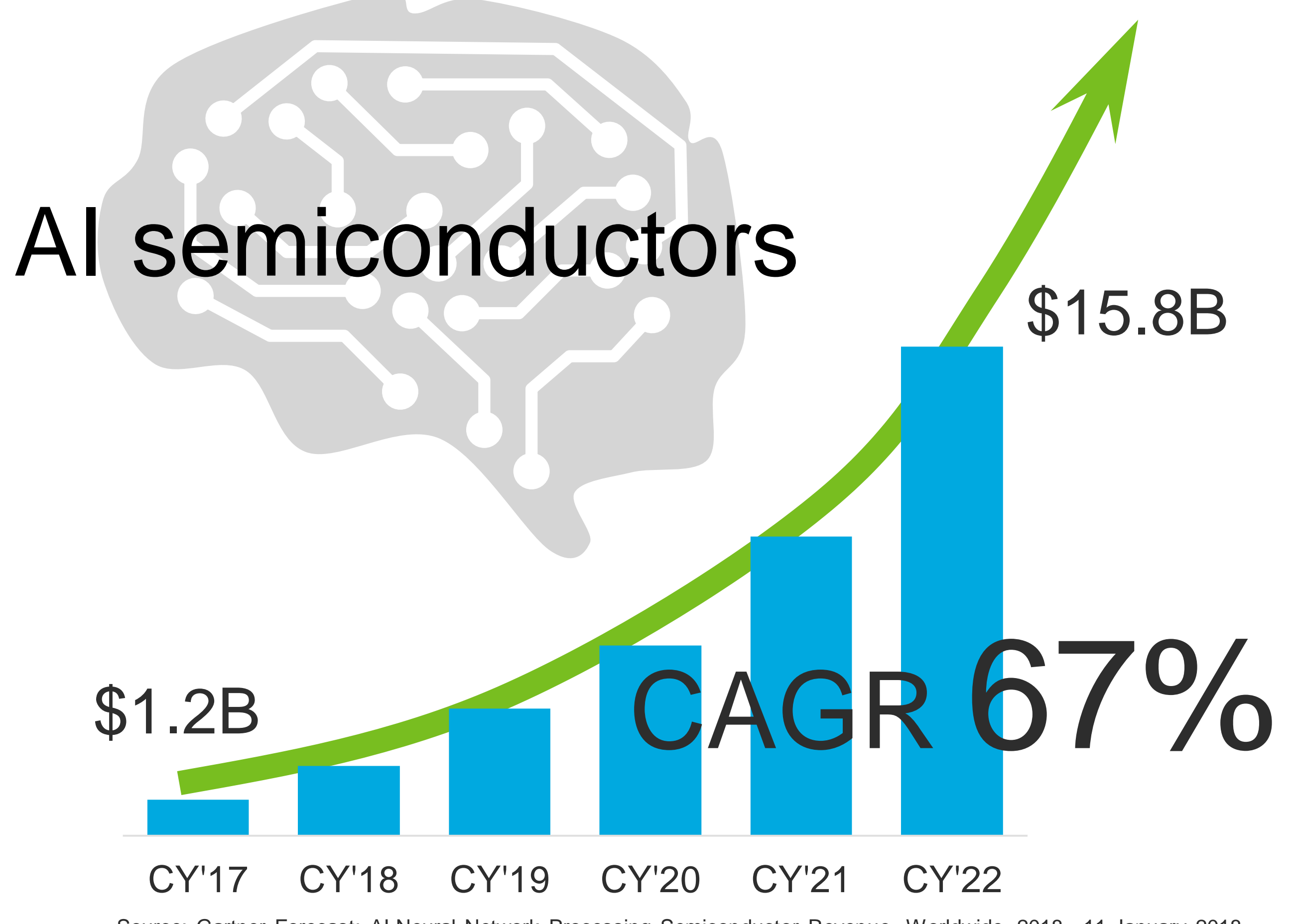


Automotive semiconductor CAGR 10.5%

Semiconductor market will continue to grow nicely in the future

 * CAGR: Compound annual growth rate

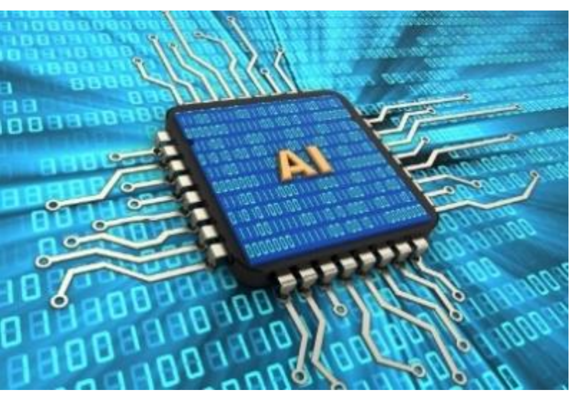
Artificial Intelligence



Source: Gartner Forecast: AI Neural Network Processing Semiconductor Revenue, Worldwide, 2018 , 11 January 2018
Charts/graphics created by Tokyo Electron based on Gartner research

Phenomenal growth rate of AI Semiconductors

AI chip development intensifying

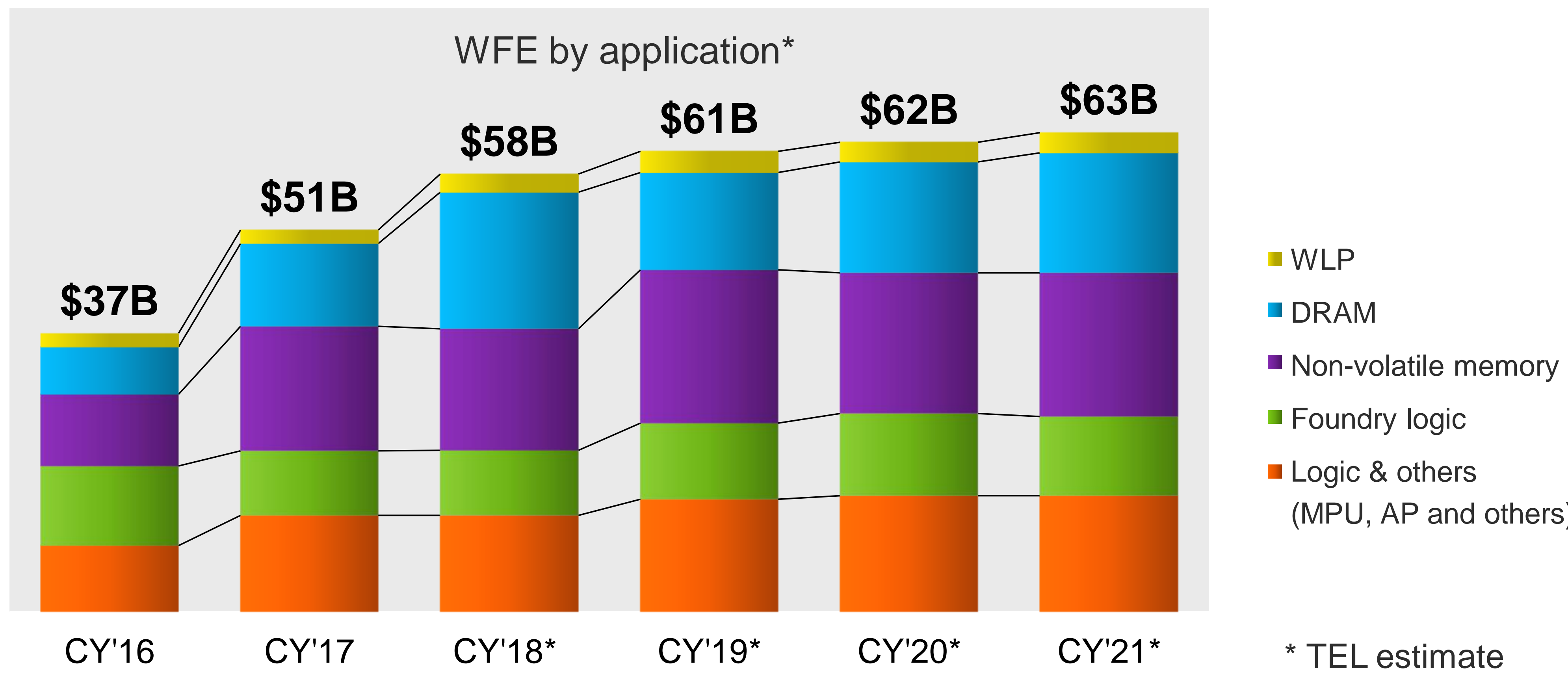


AI devices expected to grow at an annualized rate of almost 70%

Motivation for AI Chip Development

- **GPU (Graphics Processing Unit)**
  - De facto standard for deep learning today
  - But energy consumption is high and requires additional cooling mechanism
  - For loosely linked neural networks, there is inefficiencies in computation
    - Some data centers use FPGAs listed below
    - New ASICs are being developed and further evolution is needed as an accelerator
- **FPGA (field-programmable gate array)**
  - Adapts to the various deep learning calculation models and circuits can be modified flexibly
  - But computation is relatively slow (clock frequency: tens of MHz - hundreds of MHz)
  - Design hurdle is high and requires hardware knowledge
- **Neuromorphic**
  - New brain like architecture and device development is being accelerated to optimize AI application
  - Existing semiconductor processes and materials are thought to be compatible
  - Tokyo Electron Limited works with multiple partners to address AI development needs

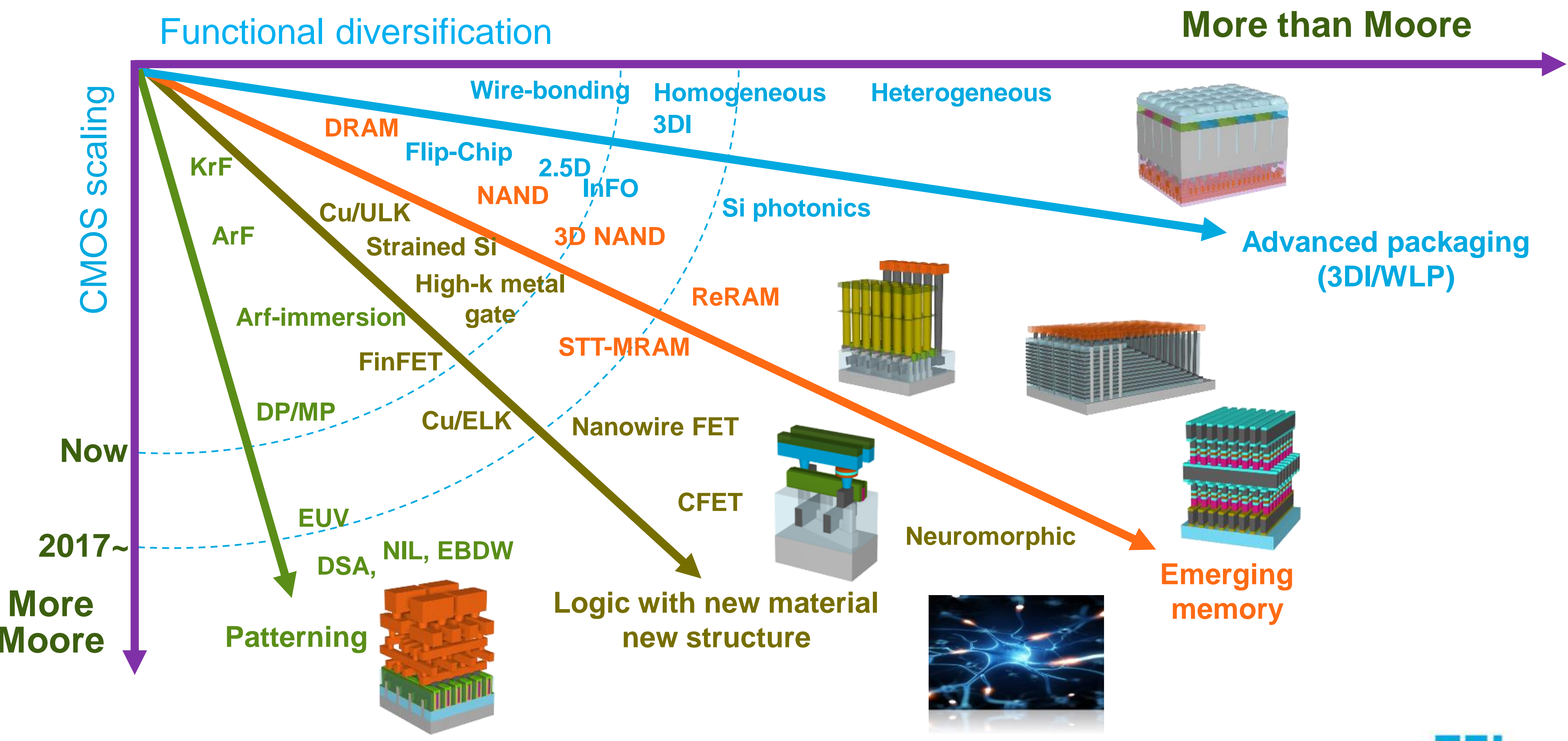
WFE Outlook



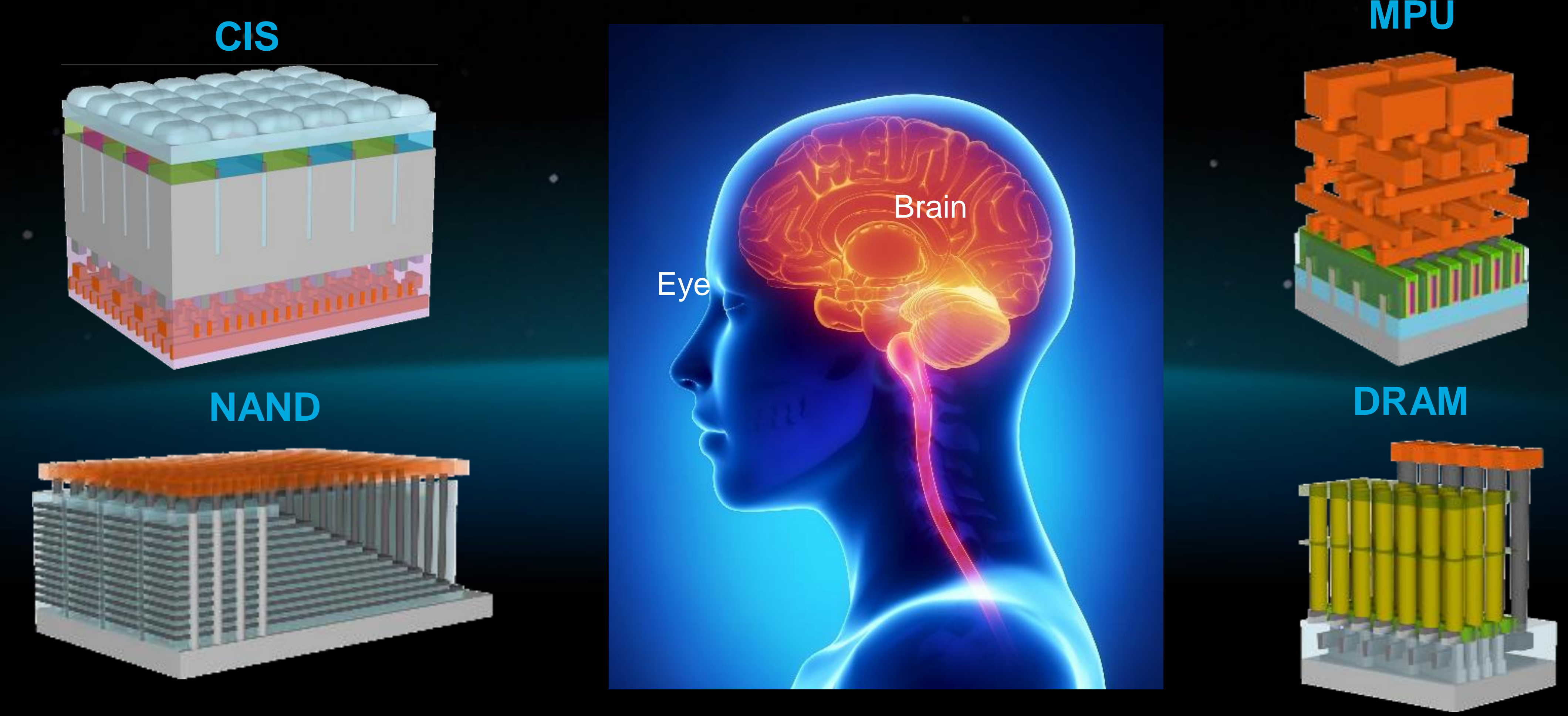
New semiconductor devices will grow WFE market over the medium- to long- term

Summary

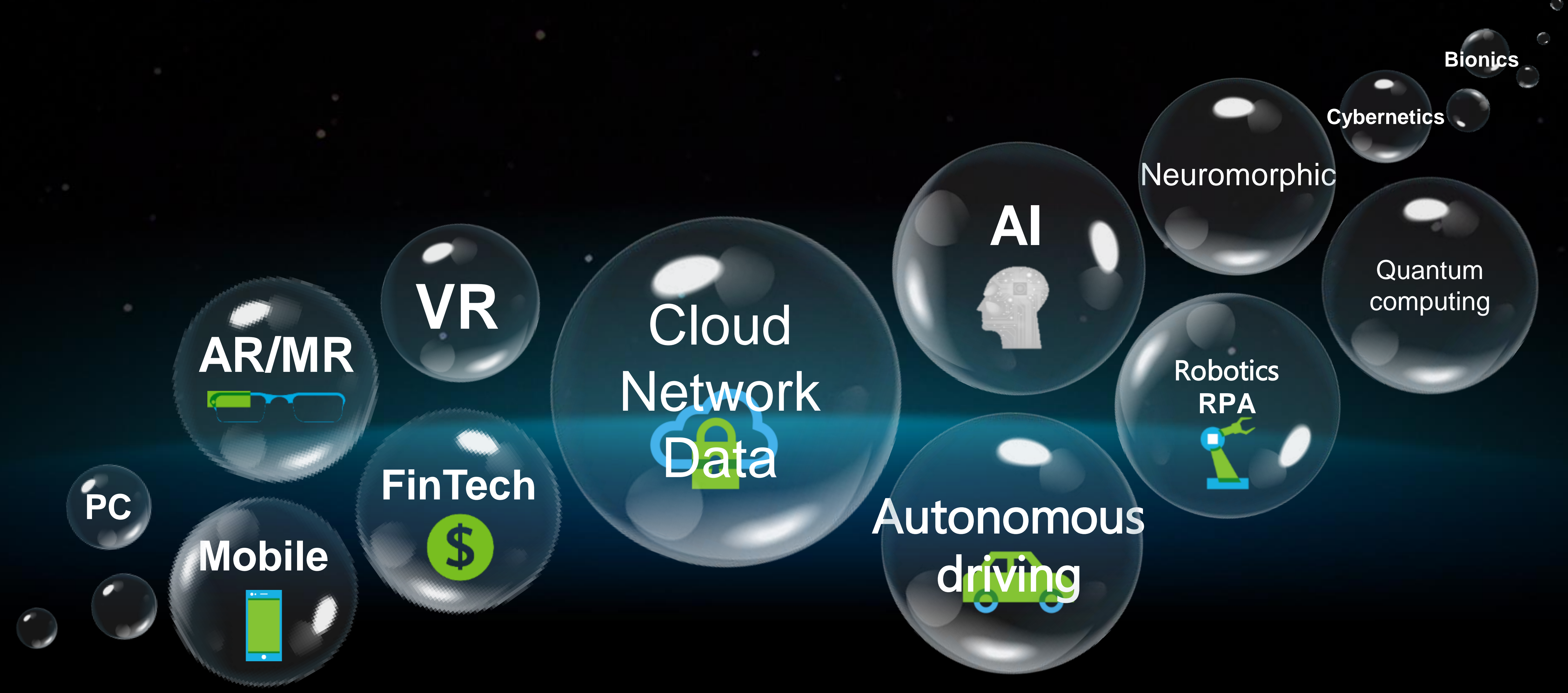
Summary – Diversity of Semiconductor Technology



Devices That Have Made Today's Technology Possible



With new devices like AI and Neuromorphic chips joining the mix, the market will continue to grow synergistically with the communication system network growth



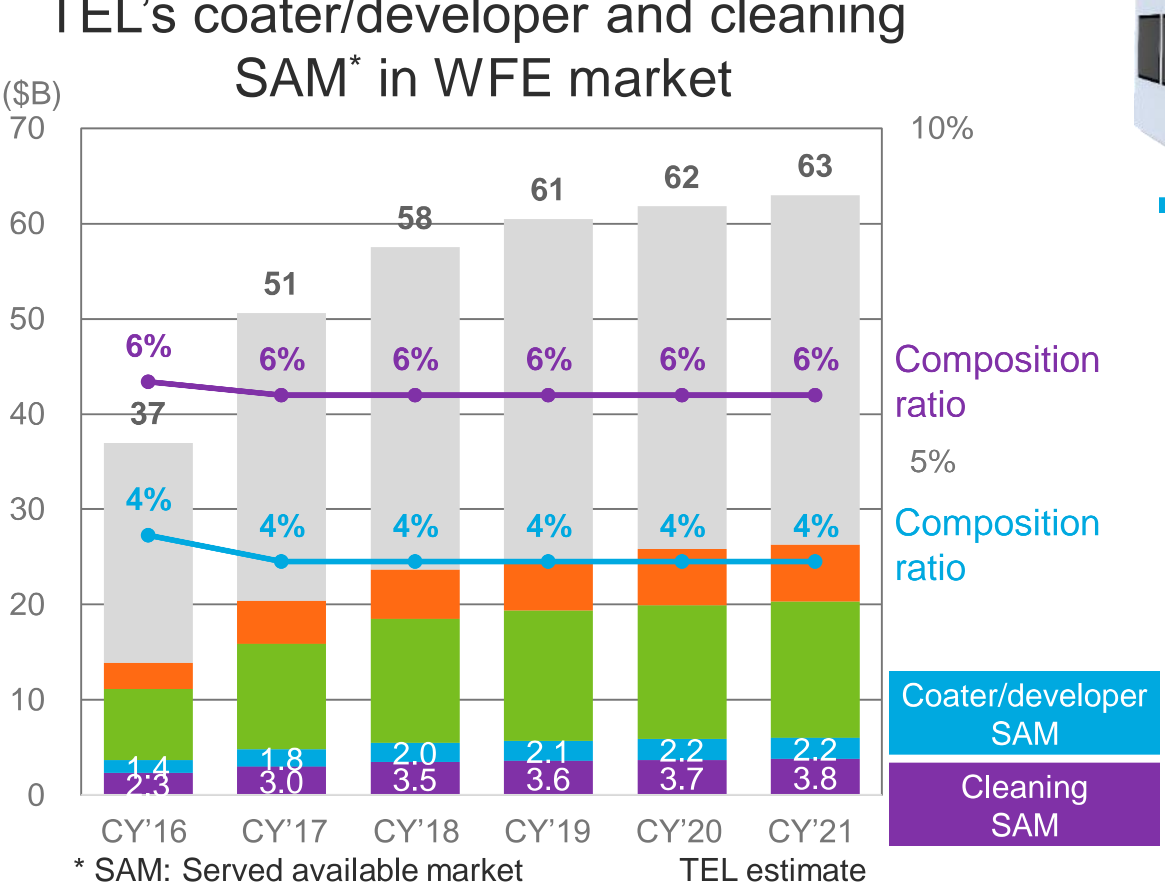
Technology Evolution at a Glance

Coater/developer, Cleaning System Business Strategy

May 29, 2018

Seisu (Yoh) Ikeda
SVP & GM, Deputy General Manager, Business Division, General Manager, CTSPS BU

Coater/developer and Cleaning Systems Market Outlook



Coater/developer
CLEAN TRACK™ LITHIUS Pro™ Z

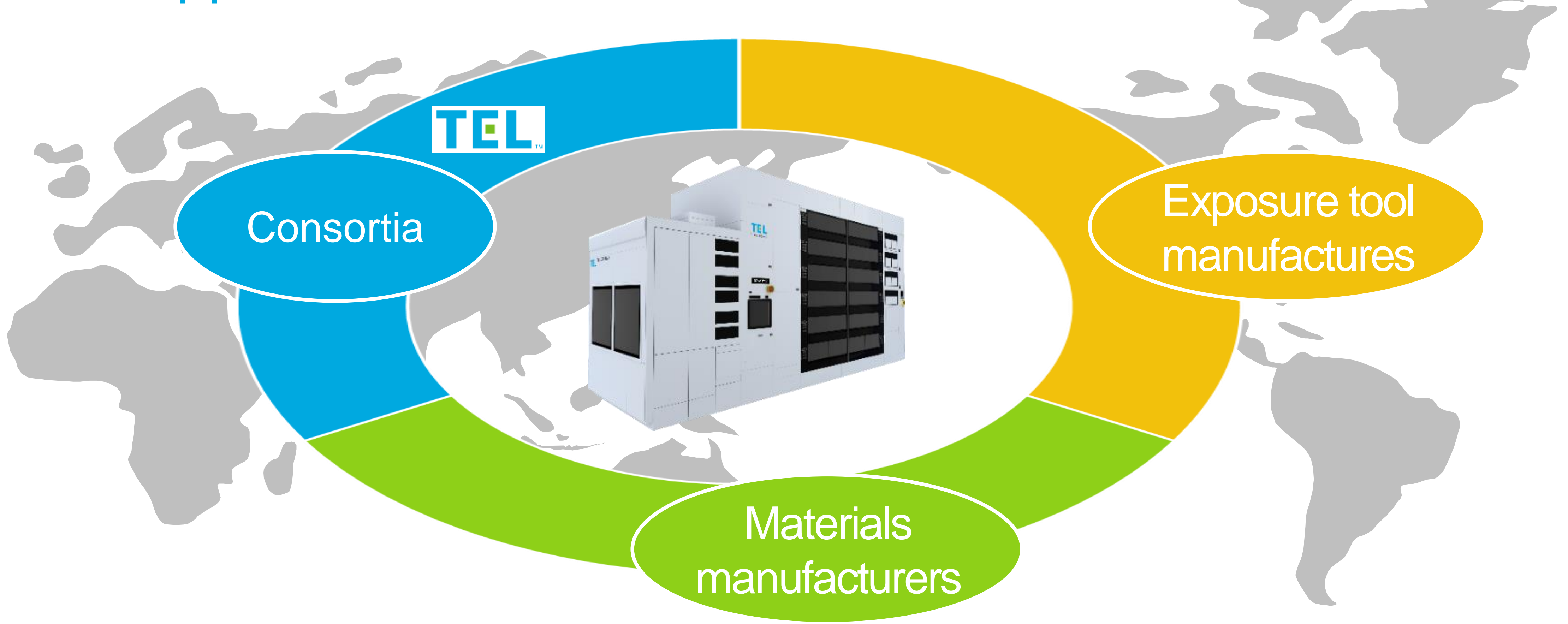
Single wafer cleaning system
CELLESTA™-*i*

Batch cleaning system
EXPEDIUS™-*i*

- Coater/developer
  - Introduction of EUV lithography for mass production
  - Established regional offices in China and expanded support for customers
- Cleaning system
  - Growth in wet etch market for 3D NAND
  - Increased demand for bevel cleaning
  - Further demand for drying technology that prevents pattern collapse accompanying miniaturization

Growth in coater/developer and cleaning systems markets on demand for increasing density of semiconductor components

EUV: Approach and Results



- Linking valuable data, customer needs, issues and information received through many collaborative businesses with development
- Maintain 100% share in EUV in-line equipment market

Continue acceleration of further EUV development

Changing Issues in Introduction of EUV Mass Production (announced at EUVL Symposium)

Priority	2014	2015	2016	2017
1	Reliable source operation with > 75% availability	Reliable source operation with > 85% availability	Reliable source operation with > 85% availability	Resist resolution, stochastics, and sensitivity met simultaneously
2	Resist resolution, sensitivity & LER* met simultaneously	Resist resolution, sensitivity & LER met simultaneously	Resist resolution, sensitivity & LER met simultaneously	Reliable source > 250W operation with > 90% availability
3	Mask yield & defect inspection/review infrastructure	Mask yield & defect inspection/review infrastructure	Keeping mask defect free	Keeping mask defect free
4	Keeping mask defect free	Keeping mask defect free	Mask yield & defect inspection/review infrastructure	Mask yield & defect inspection/review infrastructure

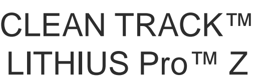
* LER: Line edge roughness

Source: 2017 EUVL Symposium Closing Remarks

Importance of resist performance and coater/developer technology increasing within EUV process

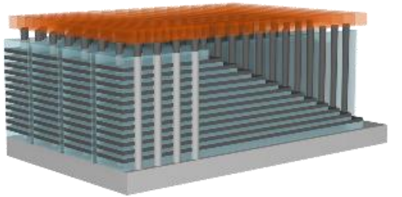
Product Strategy for Coater/developers

- Promote unification of system platforms
  - Improve value for customers and unify development with latest platform of LITHIUS Pro™ Z series
- Develop value-added products for miniaturization and 3D structures
  - Address 3D NAND wafer warpage
- Improve quality of service and efficiency through use of data and automation
  - Realize high-quality global support not reliant on technical skill of personnel

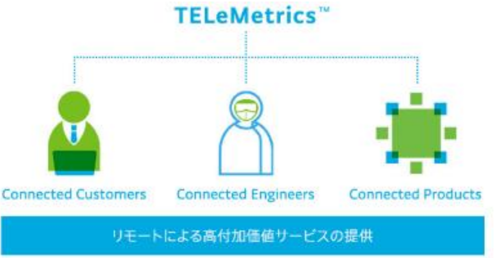


CLEAN TRACK™
LITHIUS Pro™ Z

CLEAN TRACK™
LITHIUS Pro™ AP



3D NAND



Growth of TEL's Cleaning Business

- **CY'17 market share: 25% (YoY+5pts, achieved medium-term plan early)**

Market share	CY'15 (Actual)	CY'16 (Actual)	CY'17 (Actual)	. . .	CY'20 (Target)
Cleaning system	18%	20%	25%		27%+

– **Expand sales of CELLESTA™ single wafer cleaning system**
  - Bevel cleaning*: Improved yield around extreme edge of wafer
  - Post-etch cleaning for memory: improved productivity
  - Apply best known coater/developer methods to cleaning system business
    - ✓ Share leading-edge technology and expertise by unifying development

– **Expand sales of EXPEDIUS™ batch cleaning system**
  - Contribute to improved productivity of 3D NAND
  - Improve wet etch performance and contribute to enhanced yield

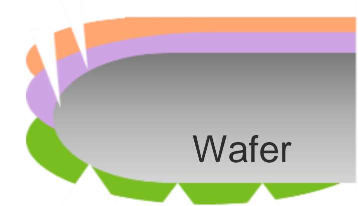
Bevel cleaning

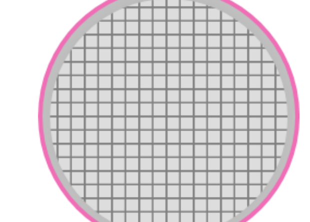
(single wafer cleaning system CELLESTA™)

Extreme edge of wafer (enlarged)

300mm wafer

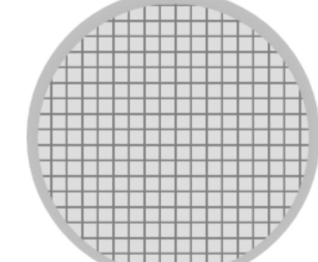
Pre-clean





Due to increasing number of films stacked on wafer, films on a wafer's extreme edge become defects, affecting yield

Post-clean



Established leading positon in developing equipment for accurate removal of film from a wafer's extreme edge, improving yield for customers

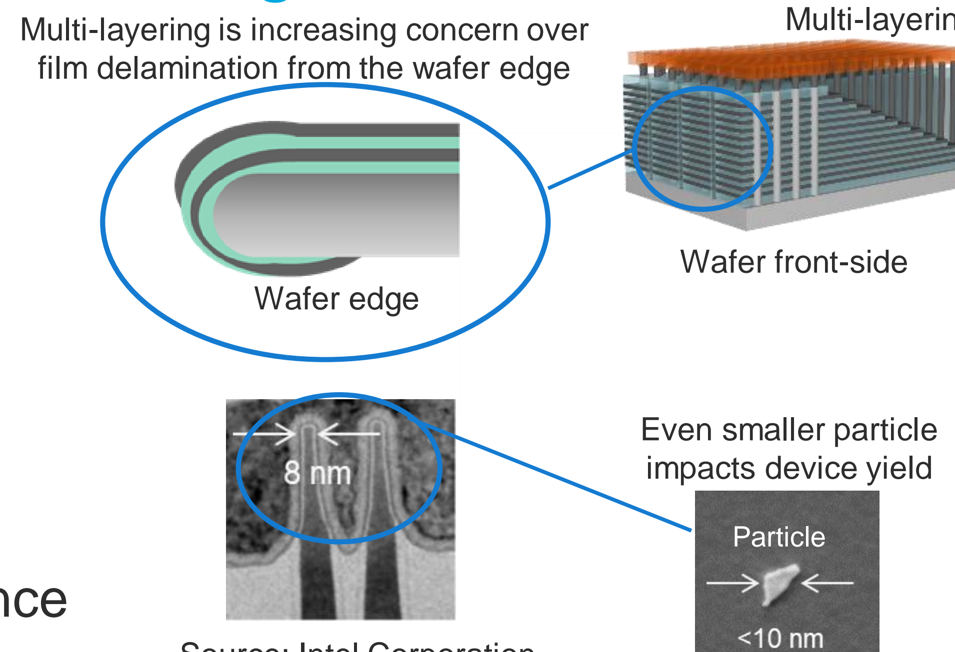
* Bevel cleaning: process for removing unnecessary film from the outer part of the wafer

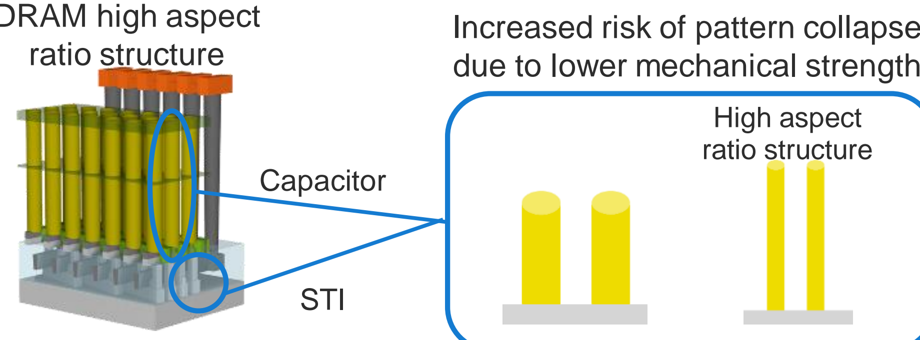
Evolving Devices: Issues and Factors Lowering Yield

- Increased impact on wafer edge due to multi-layering
  - Concern over film delaminating from edge and wafer warpage
- Impact of microscopic particle on device yield in miniaturization
  - Increase of patterning processes
  - Increase of 3D structures

Increased influence of particles

- Increased risk of pattern collapse in miniaturization
  - Increased difficulty in drying due to higher aspect ratio of device structure

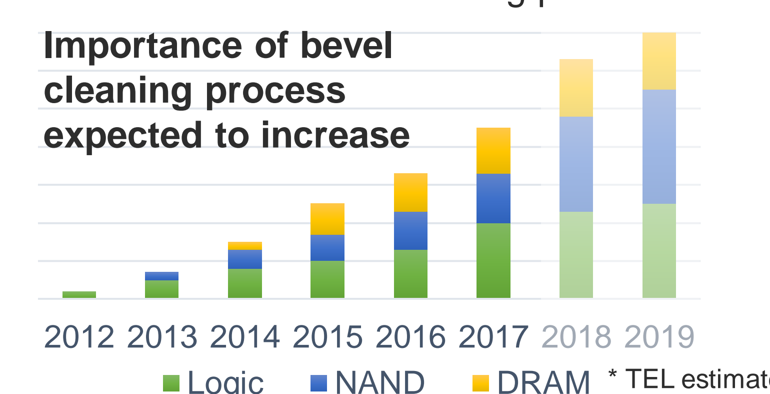




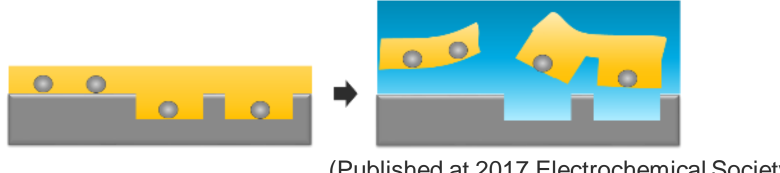
Further increase of factors reducing yield for customers on progression of multi-layering and miniaturization

TEL's Initiatives on Factors Affecting Lower Yield

- Increased impact on outer part of wafer due to multi-layering
  - Contribute to improving factors that reduce yield due to impact on wafer edge
- Impact of microscopic particle in miniaturization
  - Develop TEL original technologies enabling removal of microscopic particles and particles between patterns
- Increased risk of pattern collapse in miniaturization
  - Develop drying technology which takes advantage of TEL's original surface modification technology, etc.

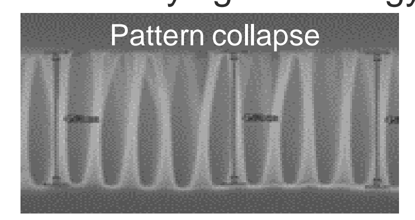


Solid phase cleaning technology (TEL original)

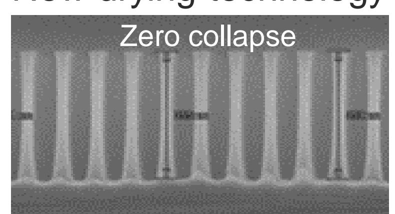


(Published at 2017 Electrochemical Society)

Current drying technology



New drying technology



Aim to further increase share by contributing to the improvement of yield for customers

Summary

- Coater/developer: Maintain high share and raise value by continuing to differentiate via technological development through collaborative activities in leading-edge technology sectors, especially EUV
- Coater/developer: Maintain high share and enhance our ability to support customers in China, where the market is growing rapidly
- Cleaning system: Continue to differentiate via technological development, focusing on processes where customers need a high level of technological support, such as improving yield
- Synergies: Raise efficiency of development and production by sharing BKM* and promoting unification of development, production and management of coater/developer and cleaning systems

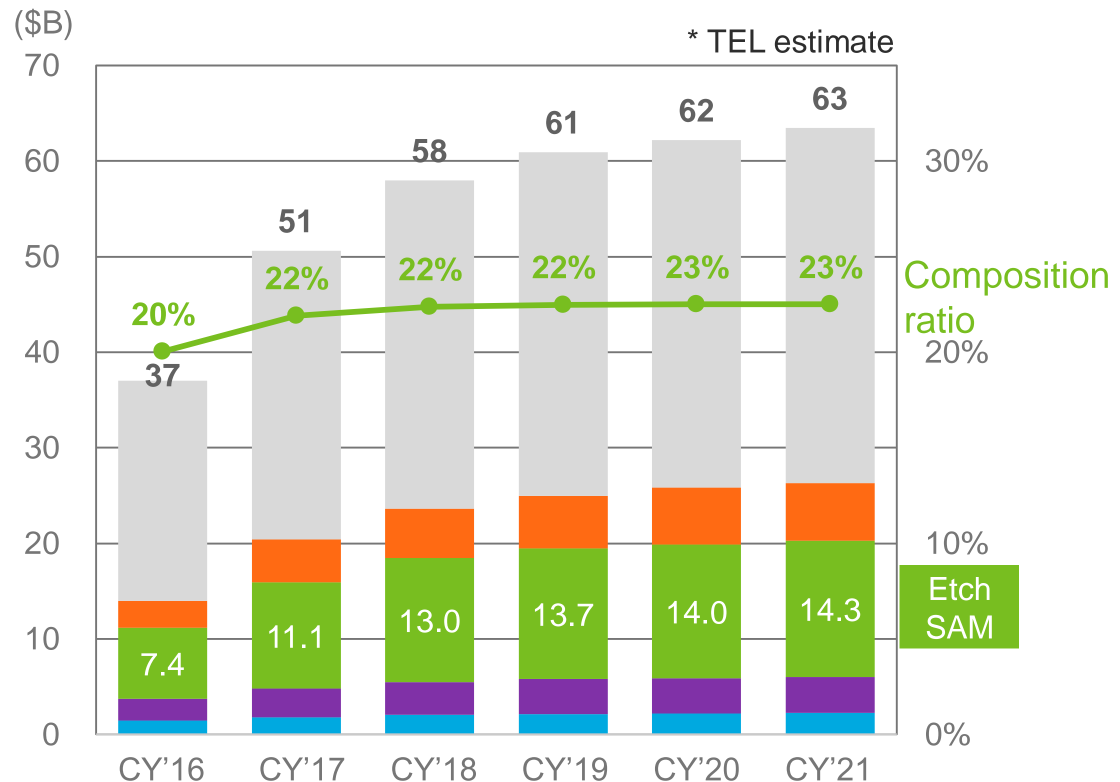
* BKM: Best known method

Etch System Business Strategy

May 29, 2018

Yoshinobu Mitano
SVP & GM, General Manager, ES BU

Etch System Market Outlook



Tactras™ Vigus™

Certas LEAGA™

Trends in etch technology

- Miniaturization of DRAM
  - Increases in patterning and copper interconnect processes
- Multi-layering of 3D NAND
  - Higher ratio of HARC* process
- Miniaturization and greater structural complexity of logic
  - Increases in patterning processes, isotropic etch

* HARC (High aspect ratio contact) process: a process for forming deep holes that requires advanced processing technology

Growth in etch system market due to increase in patterning processes and greater structural complexity

TEL

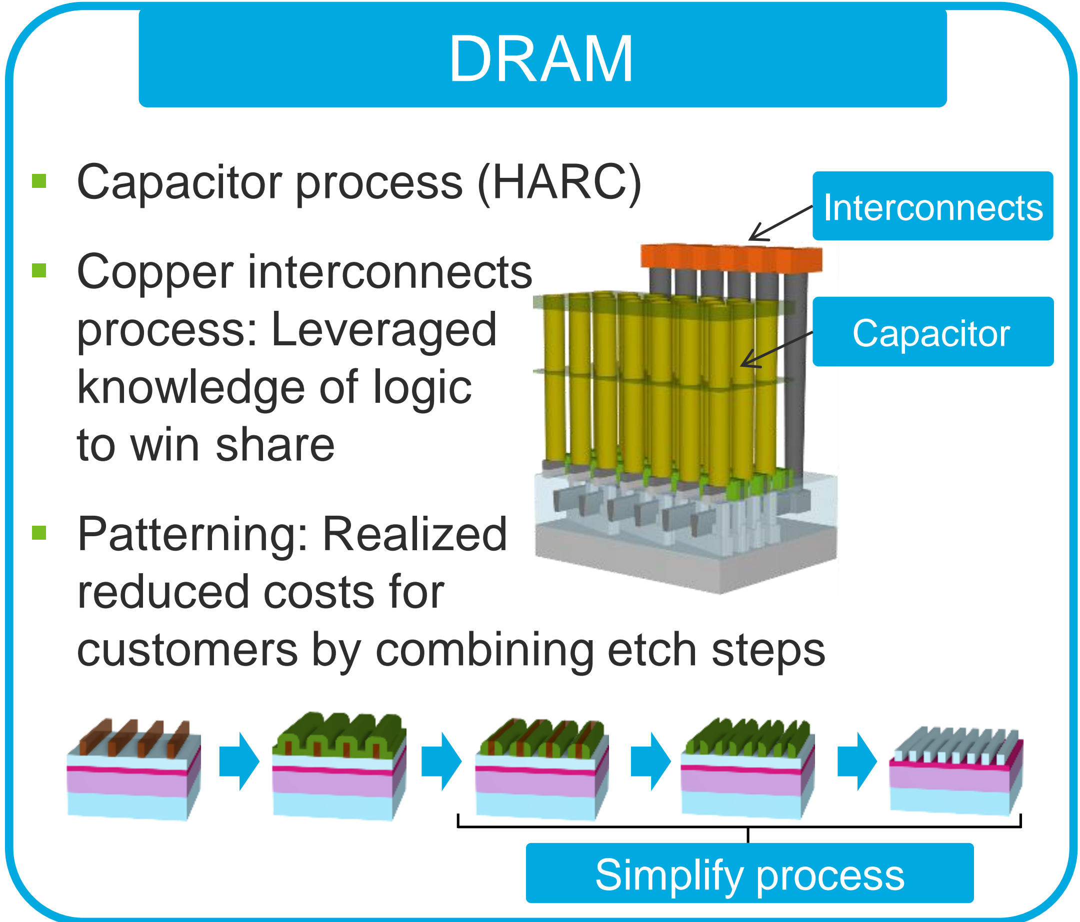
Business Opportunities and Strategy

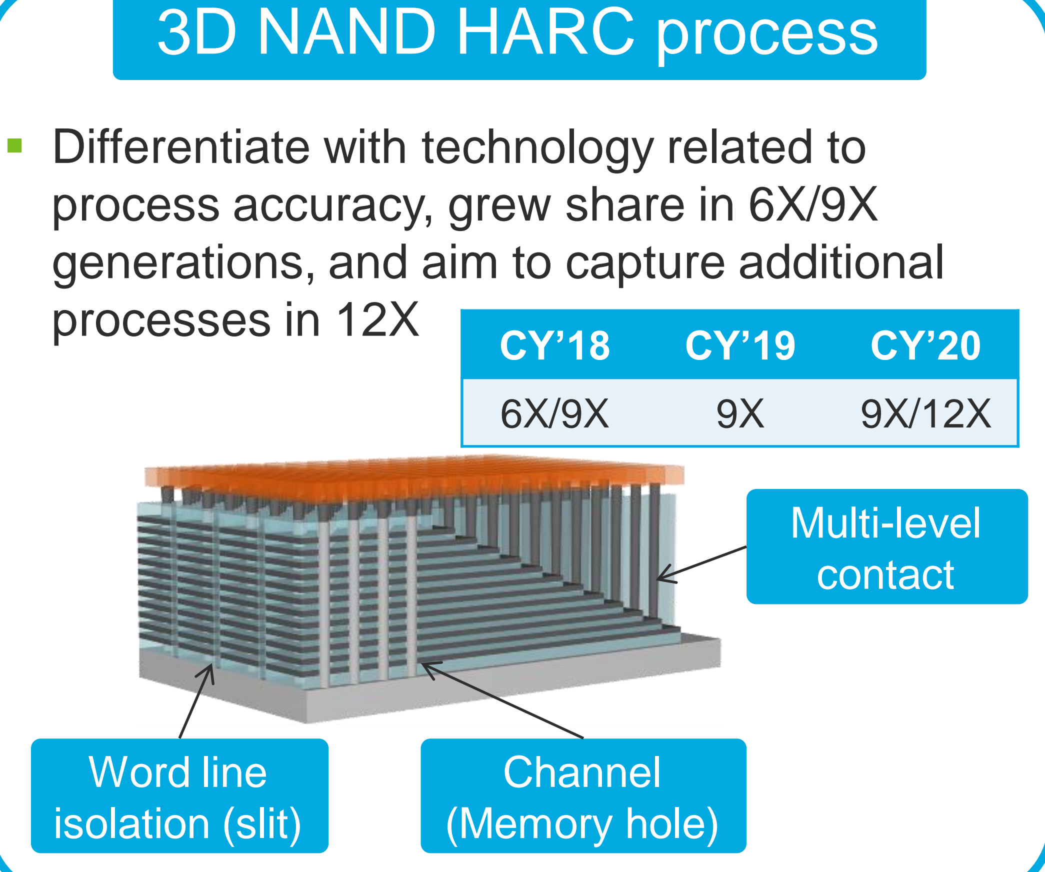
- Win share and raise profitability by leveraging technological advantage
  - DRAM: Win share in patterning process, etc. through productivity differentiation
  - NAND: Win share in new HARC process through technological differentiation
  - Logic:
    - Leverage RLSA™ plasma silicon etch to drive sales growth in transistor periphery processes
    - In contact processes, aim to increase share with atomic layer etch (ALE)
    - In 3D transistors, capture share with isotropic etch
- Grow sales through proactive development and investment in production

Market share	CY'15 (Actual)	CY'16 (Actual)	CY'17 (Actual)	・・・	CY'20 (Target)
Etch system	21%	23%	26%		30%+

Focus on HARC, patterning, 3D structure processes, aim for 30%+ share by CY2020

Memory: Results and Initiatives

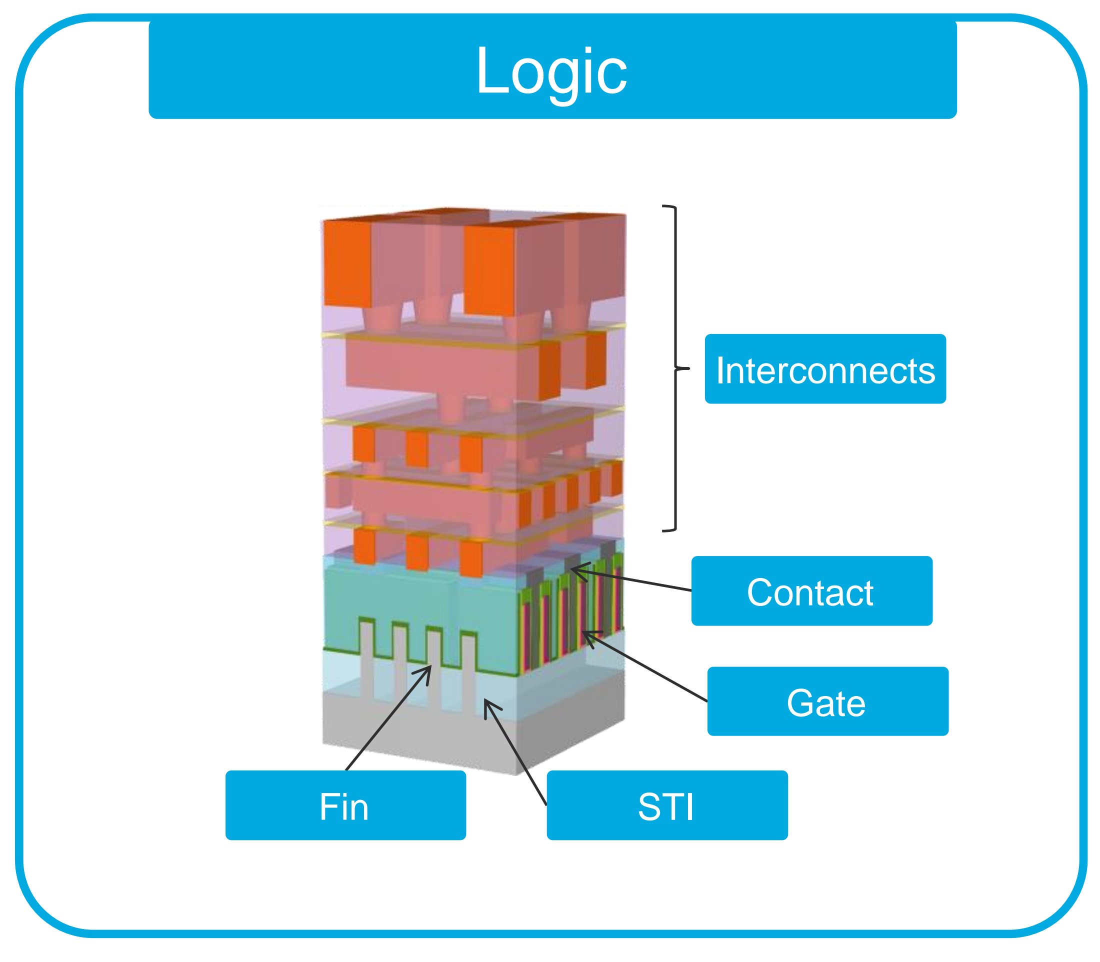




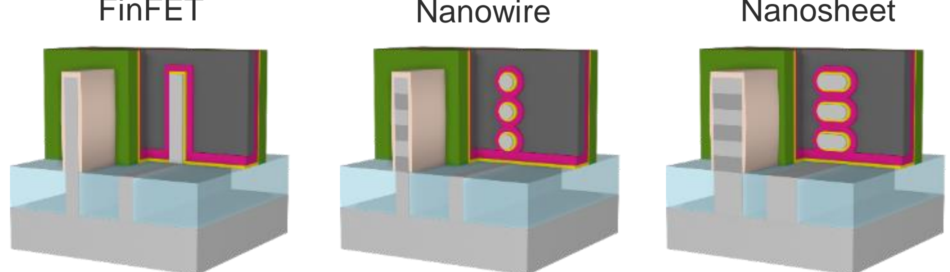
DRAM: Won share in target areas, doubling share from 3 years ago

NAND: Won application from second customer in slit process.
Aim to leverage new technology to increase POR wins

Logic: Focus Processes and Key Points

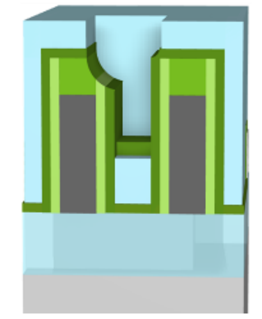


- Transistor periphery 3D structures



- Miniature contact process

SAC (Self-aligned contact)



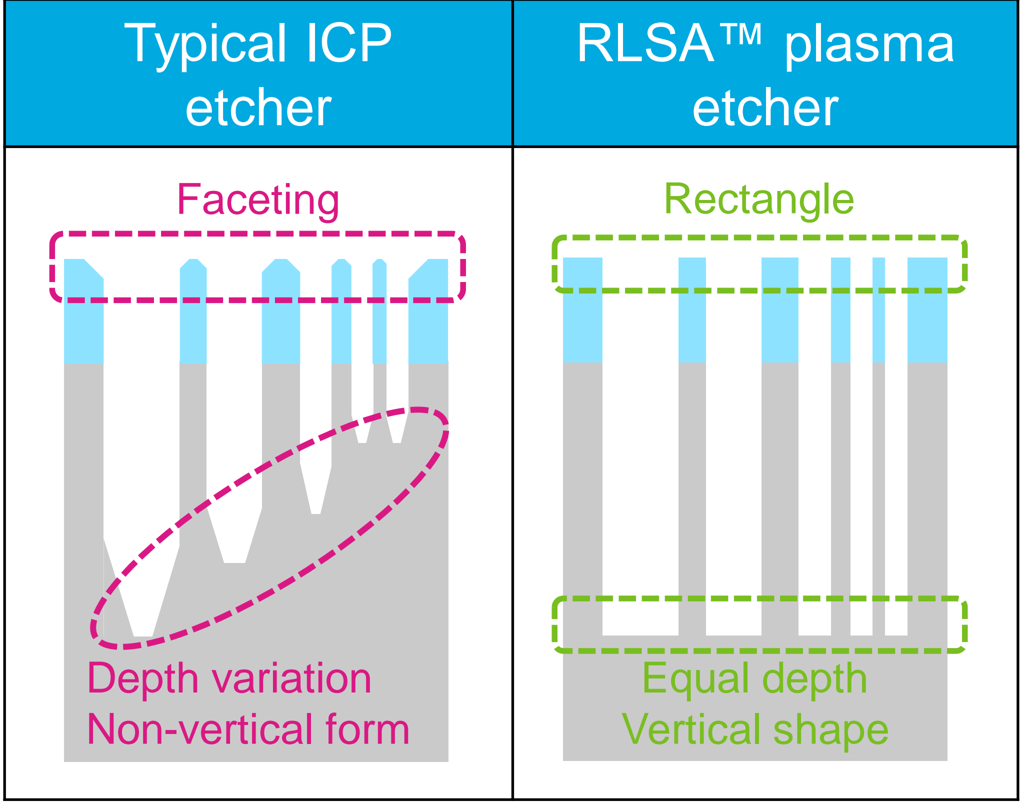
Key requirement
1. High SiN selectivity (less SiN loss)
2. Narrow slit etch capability

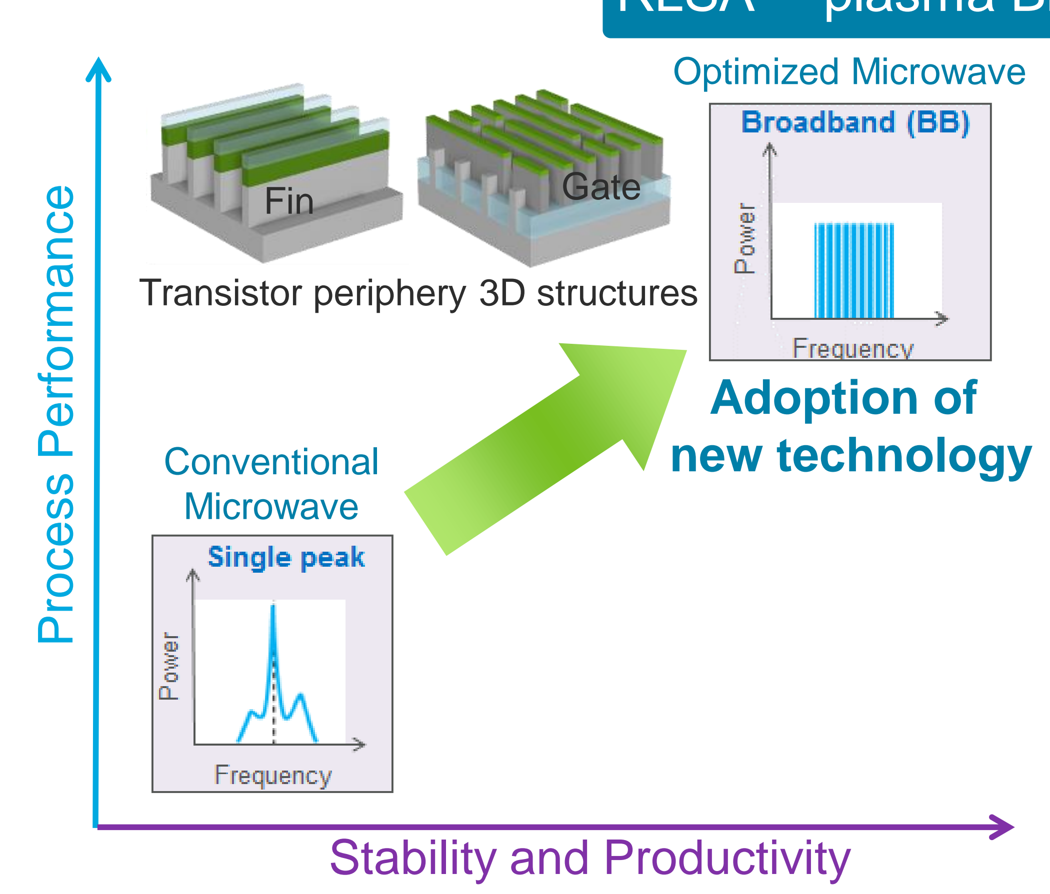
- Contact/interconnect process; more complex patterning

Leverage technological advantage in increasingly complex etch processes, respond to new needs

Leading-edge Logic Initiative 1: Silicon Etch

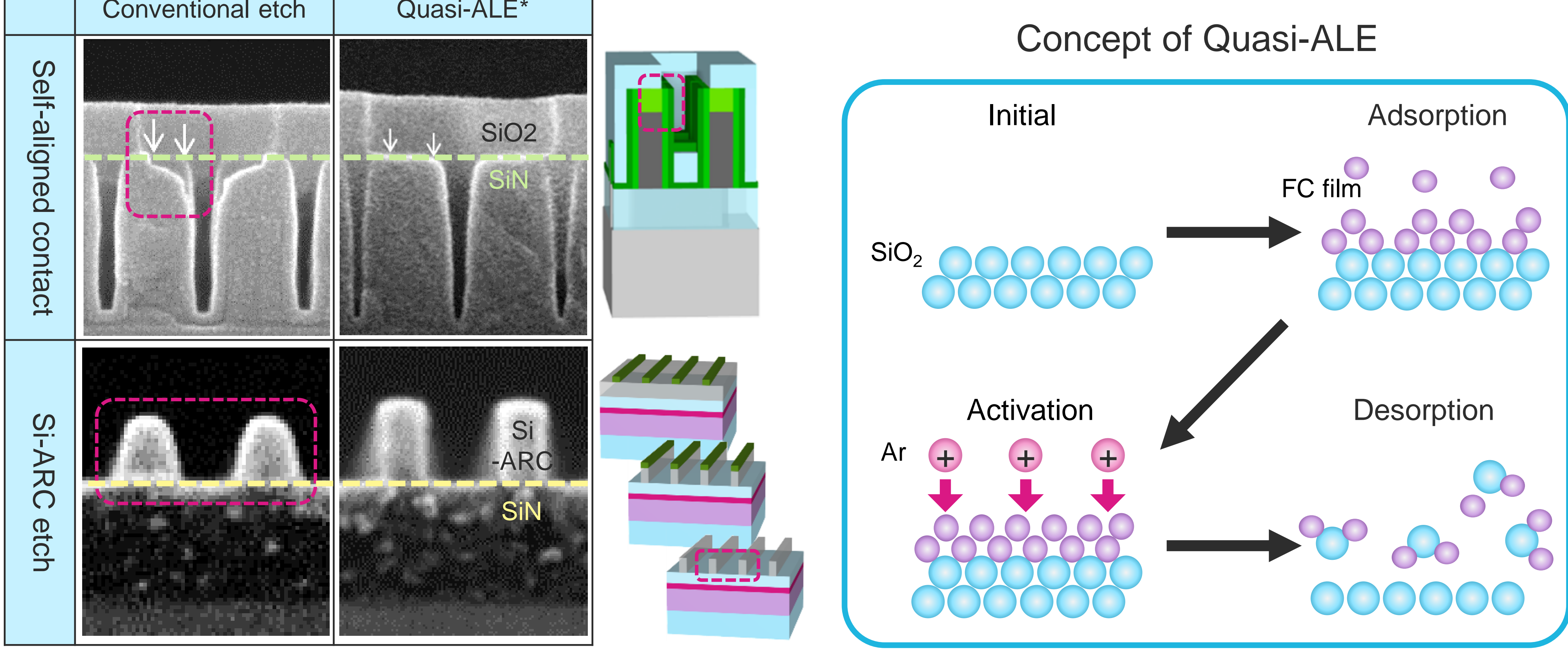
Superior aspects of RLSA™ plasma etcher in silicon etch





In silicon etch, differentiate through processing performance and productivity

Leading-edge Logic Initiative 2: Highly Selective Etch

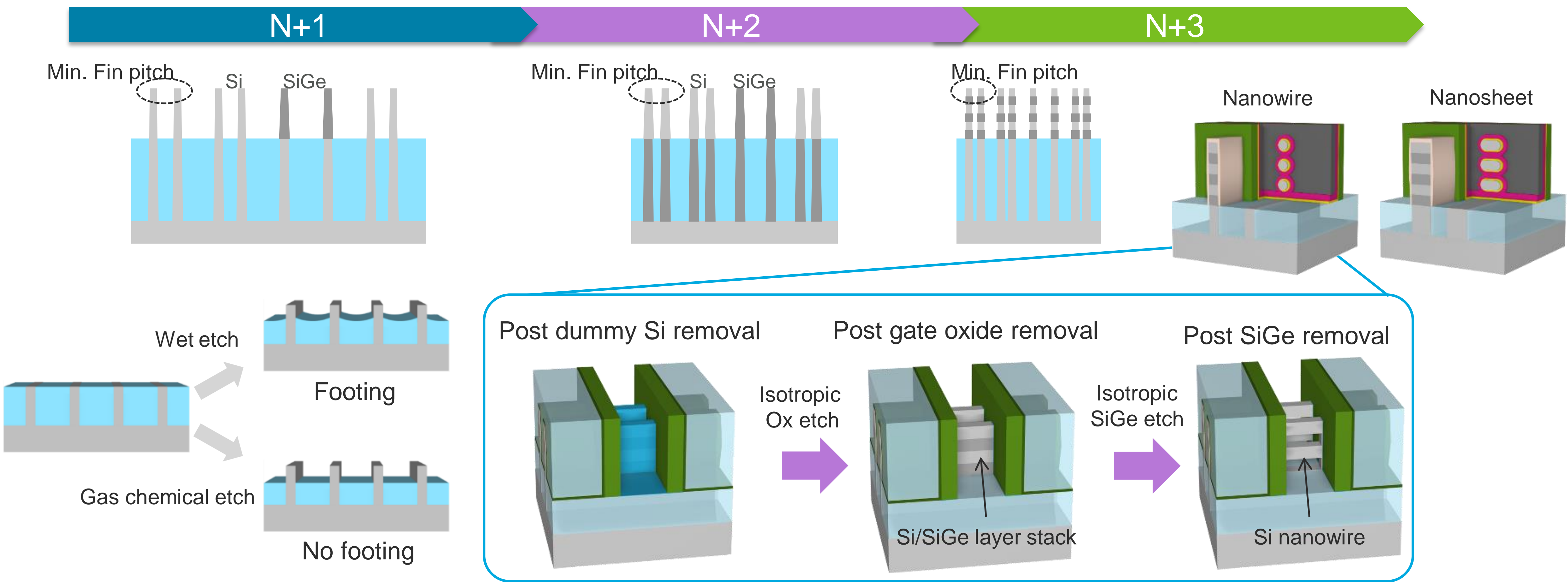


*ALE (Atomic layer etch): Highly selective etch technology at the atomic level

Aim to win share through rising demand for highly selective etch

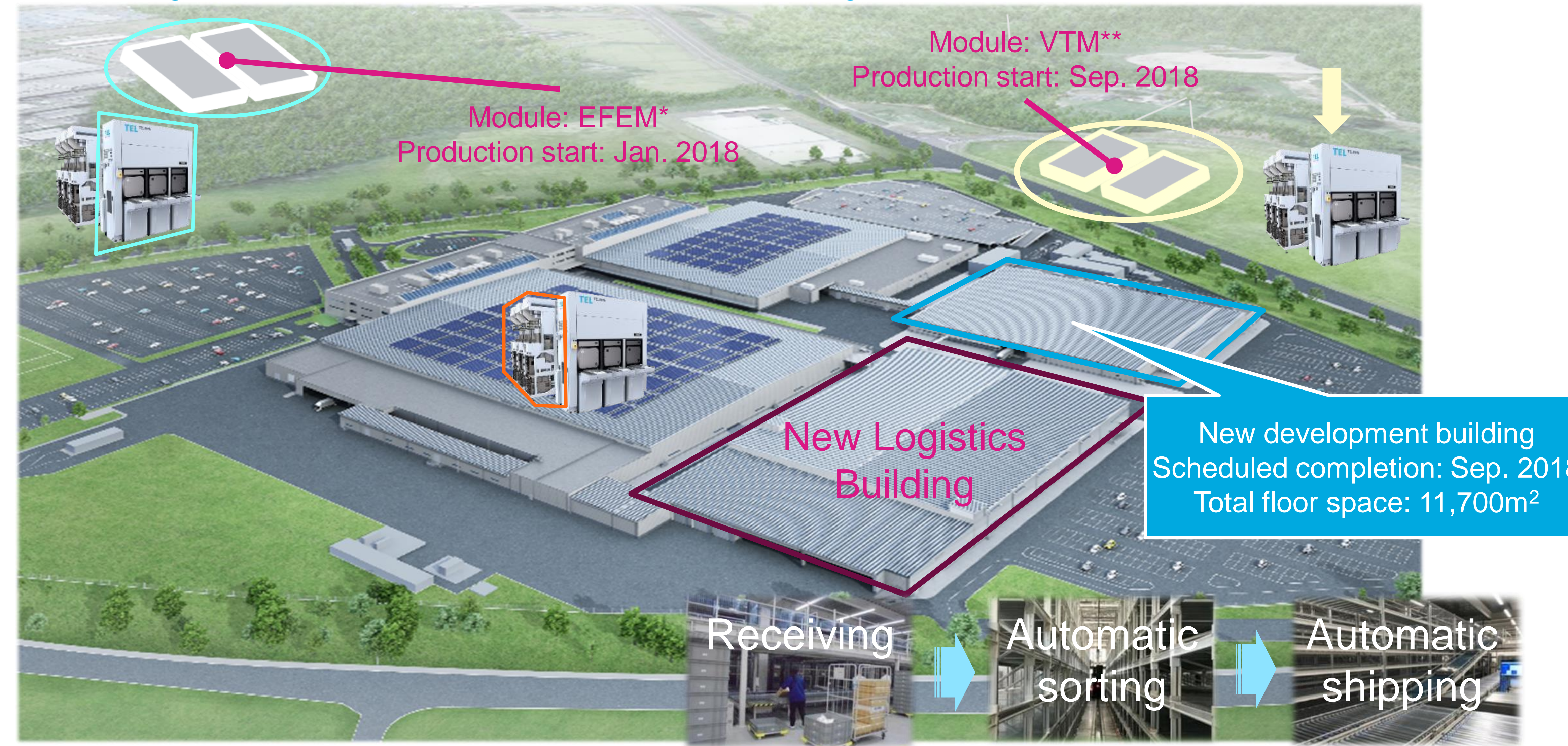
Leading-edge Logic Initiative 3: Gas Chemical Etch

Broadening of applications for gas chemical etch



Differentiate through isotropic selective etch technology needed for 3D transistors

Miyagi Plant: New Logistics Building and Module Assembly and Shipping, New Development Building



* VTM (Vacuum transfer module): Module that sends wafers to etch chamber
** EFEM (Equipment front end module): Module that moves wafers from FOUP/load ports to VTM

Summary

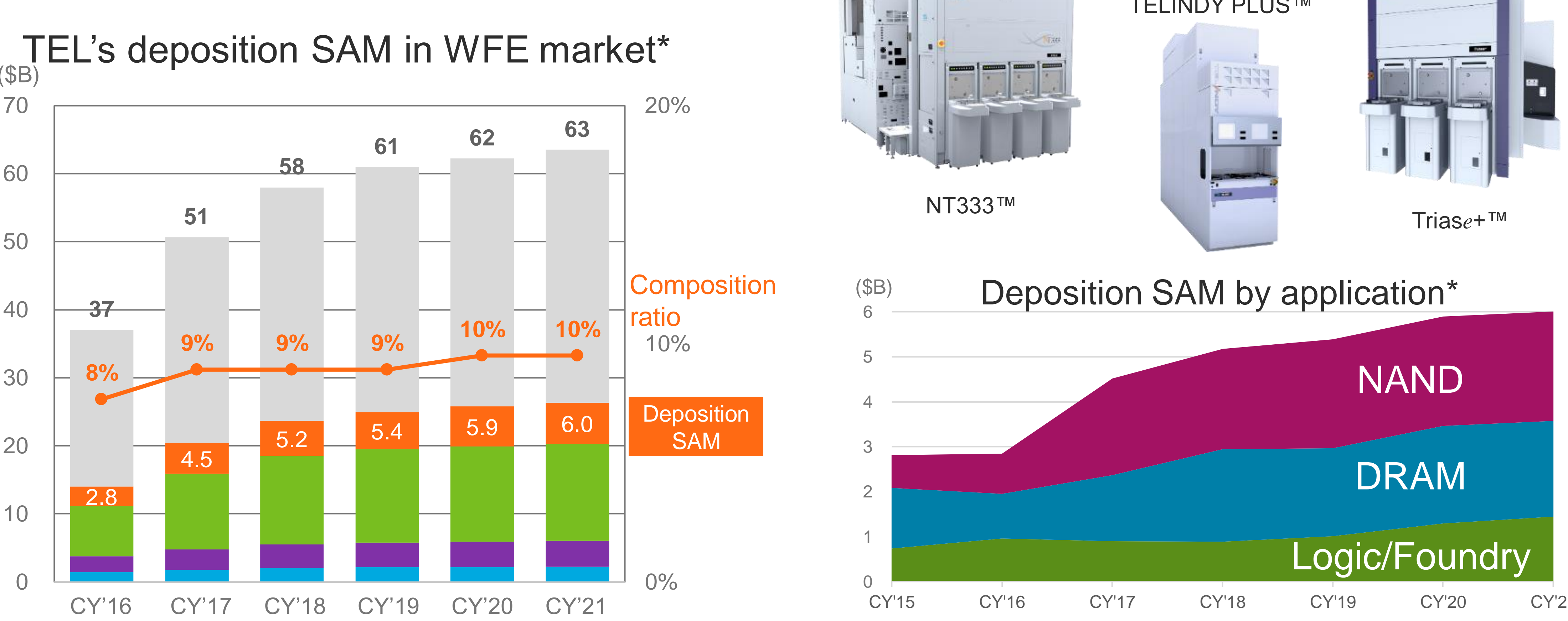
- Expect continued growth in the etch system market driven by multi-layering of 3D NAND and increasing complexity in logic patterning
- Aim to raise profitability by focusing on TEL's strengths in HARC, patterning, interconnects, achieving share of 30%+ in CY'20 through technological differentiation
- We will proactively invest towards further market growth

Deposition System Business Strategy

May 29, 2018

Shingo Tada
VP & GM, General Manager, Thin Film Formation BU

Deposition System Market Outlook



Miniaturization and evolving device structure are driving growth of the high value-added deposition market

* TEL estimate

Business Opportunities and Strategy

- In areas where we already participate in the deposition market (ALD, CVD and diffusion furnaces), introduce technology with high added value and outperform market growth
  - introduce next generation thermal processing systems with higher productivity and controllability
  - Introduce new single wafer platform for cluster process
- Accelerate development of new materials, new applications
  - Evaluate new materials for metal deposition systems
  - Develop anisotropic deposition and selective growth process

Market share	CY'15 (Actual)	CY'16 (Actual)	CY'17 (Actual)	・・・	CY'20 (Target)
Deposition system	38%	37%	36%		40%+

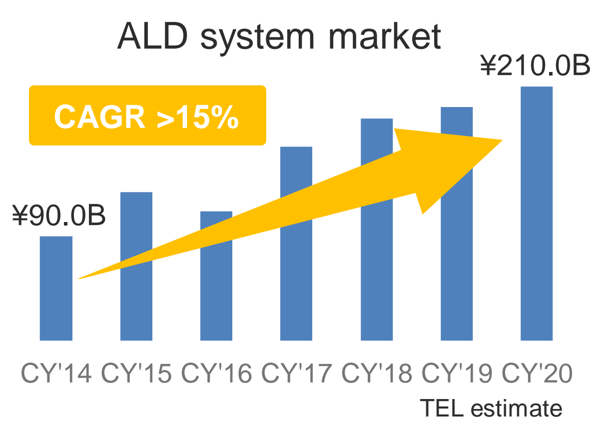
Focus on high value added deposition processes, aim for 40%+ share in CY2020

Approach to Deposition Market

ALD system

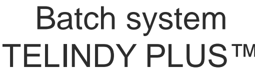
- In semi-batch systems, make high quality film required for miniaturization and shift to 3D structure, and raise productivity

Semi-batch ALD system
NT333™



CVD system

- Use our huge productivity advantage in batch systems to differentiate in memory
- Achieve high quality metal deposition to enable further miniaturization

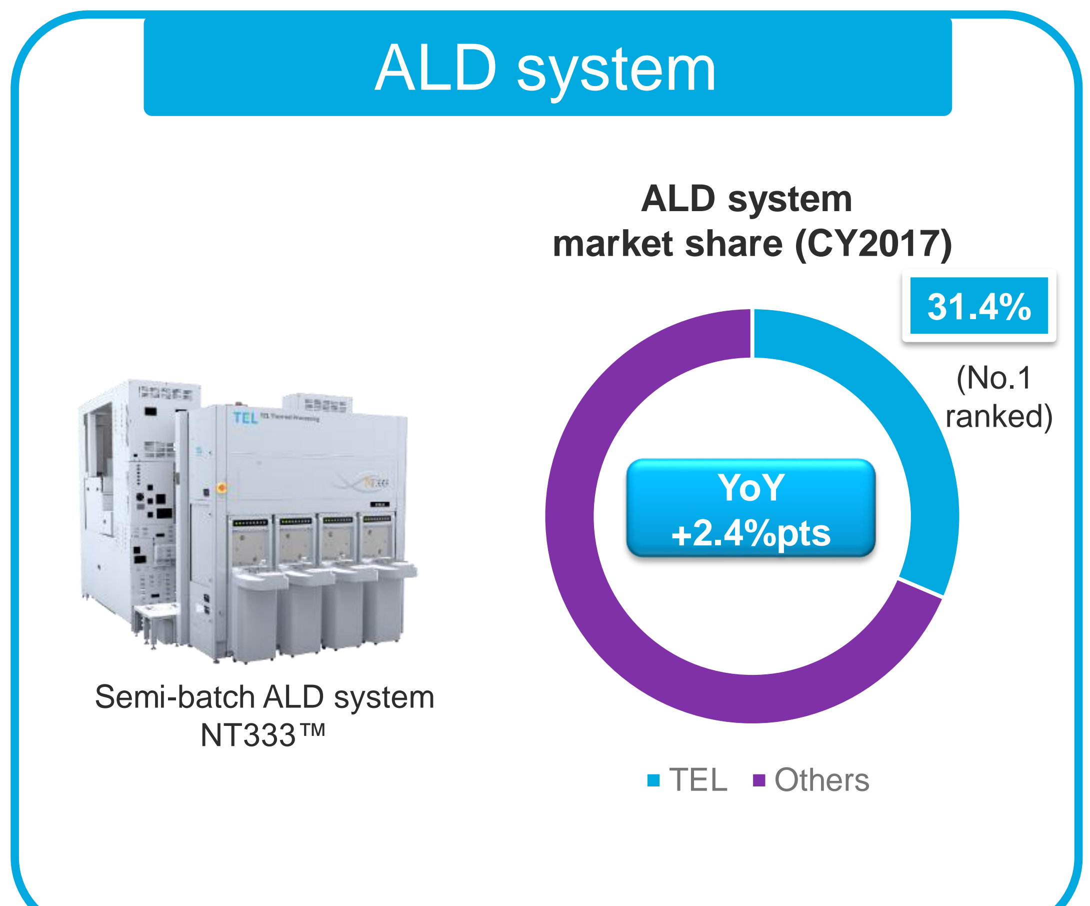


Batch system
TELINDY PLUS™

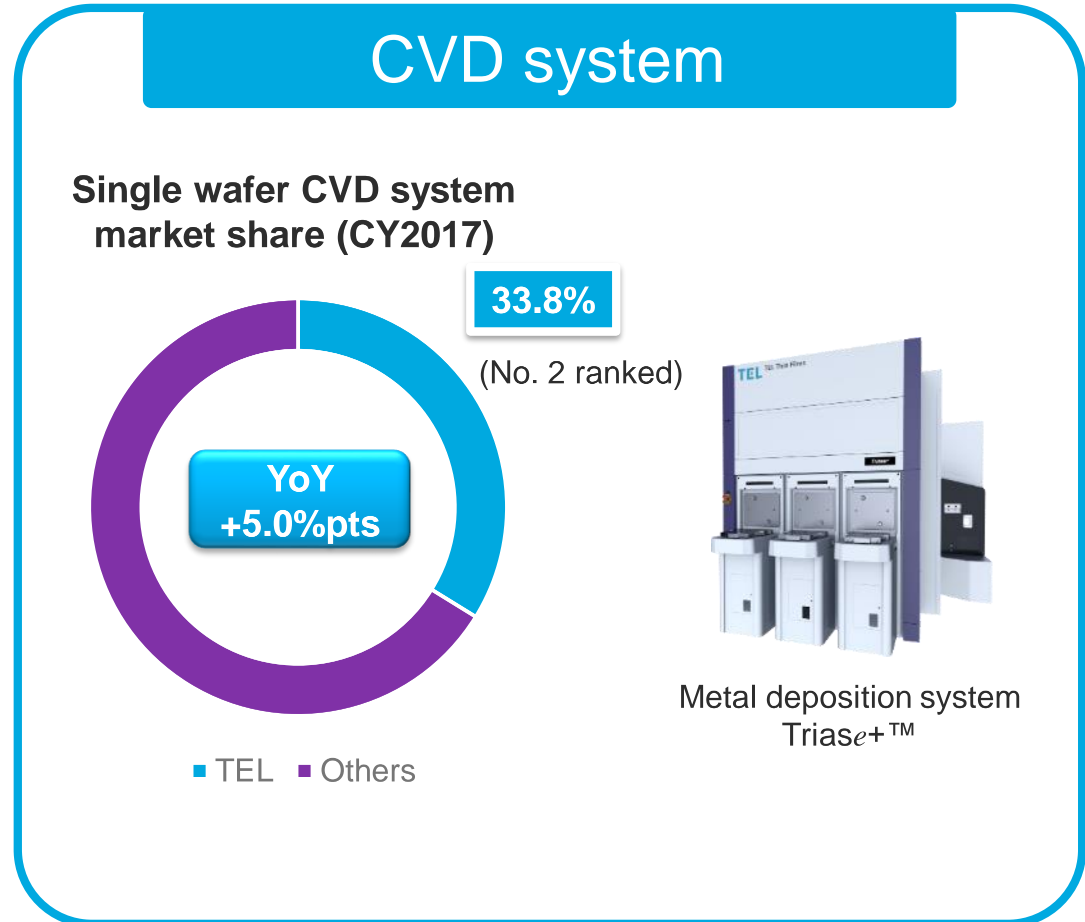
Metal deposition system
Triase+™

Aim to grow profit through and new technology for further miniaturization and next-generation semiconductors

Initiatives in the Deposition Market



Semi-batch ALD system
NT333™

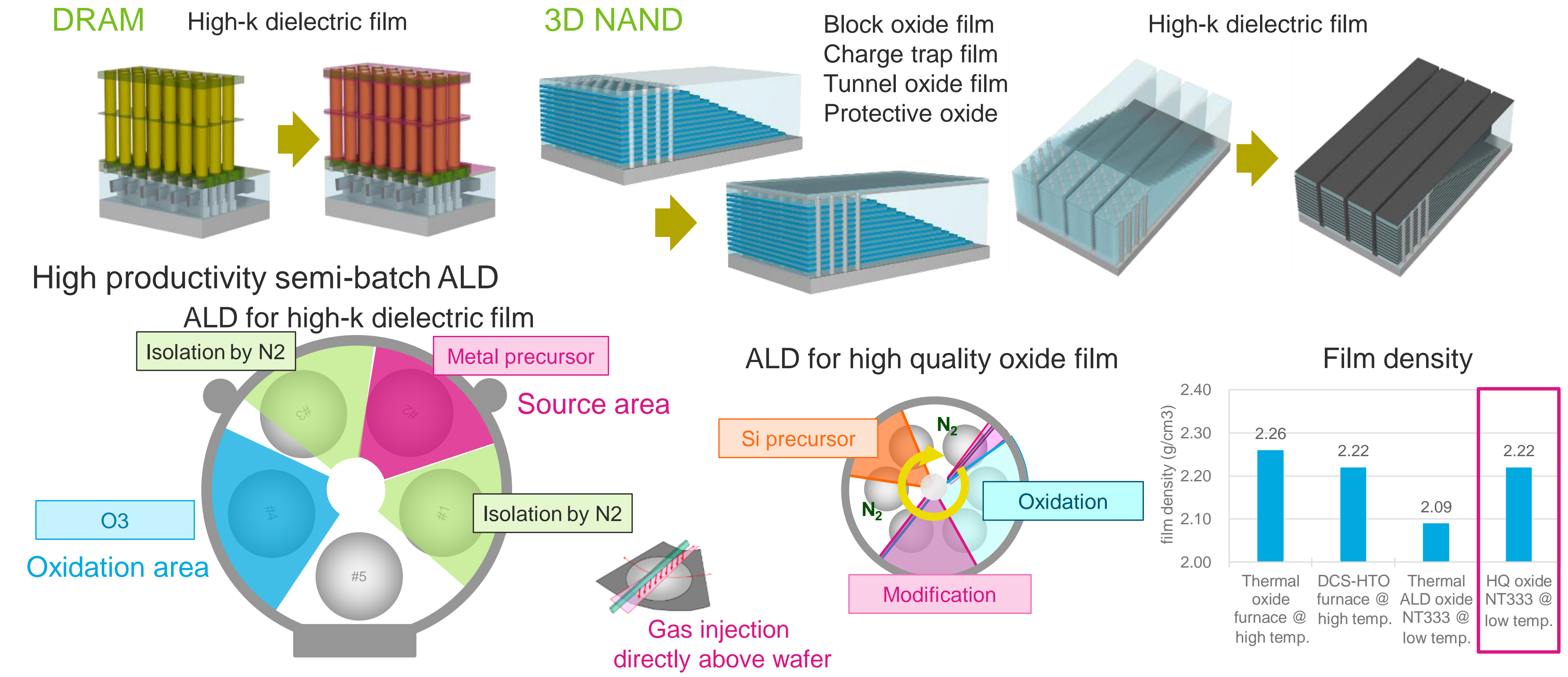


Metal deposition system
Triase+™

Source: ALD system market share=Atomic layer deposition, Single wafer CVD system market share=Nontube LPCVD, Gartner, "Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2017", 18 April 2018,
Chart created by Tokyo Electron based on Gartner research.

Focus on growing share in market segment expanding due to miniaturization

Dielectric Film Deposition Technology for High Aspect Ratio Structure



Realized high productivity deposition technology that forms high quality, uniform dielectric film without pattern dependence

TEL

Metal Deposition Technology for High Aspect Ratio

DRAM

Bottom electrode deposition

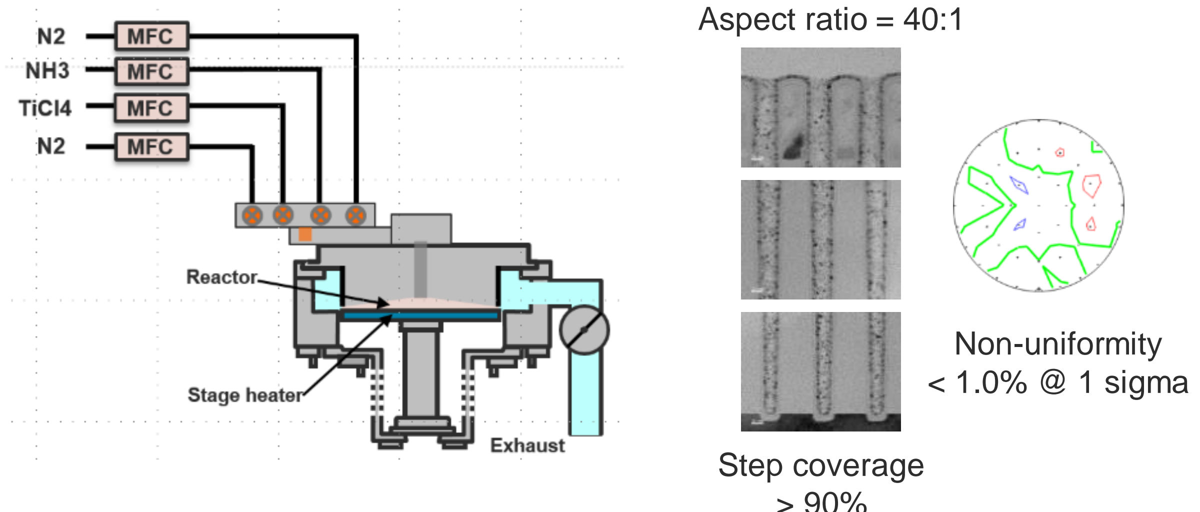
Upper electrode deposition

3D NAND

Word line, contact barrier deposition

ASFD：Advanced sequential flow deposition

- ✓ High throughput
  - Minimizes chamber volume
  - High speed, high concentration gas injection system
- ✓ Uniformity
  - Symmetrical gas flow design



Optimized deposition chamber design for ASFD provides high performance and high productivity

TEL

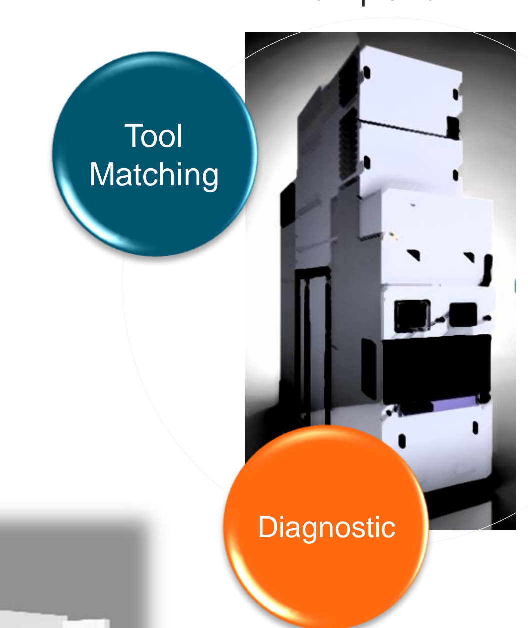
Deposition Systems: Striving for Further Growth

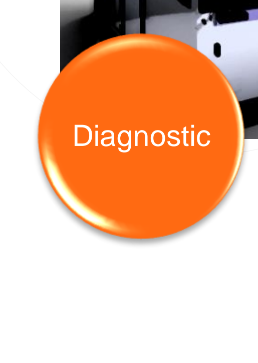
- Next generation thermal processing system
  - Introduce SLB* product with high productivity and efficiency
  - Adoption of new, high precision controller will contribute to enhance tool matching and increasing uptime

* SLB: Super large batch

- New single wafer platform
  - Smaller footprint, higher productivity
  - Enables diverse cluster processes

New platform



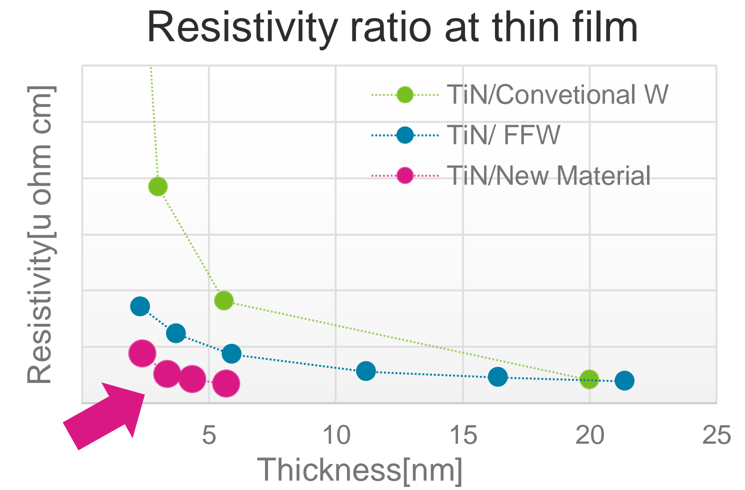


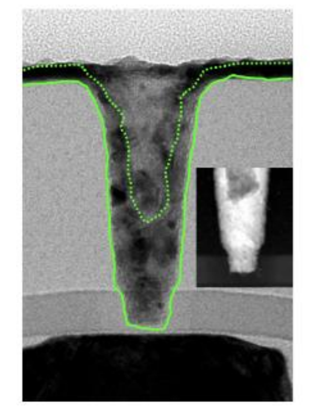
New platform

Expand market share in areas where we already participate in by increasing productivity and responding to diverse process needs

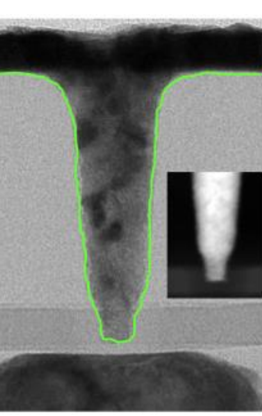
Deposition Systems: Initiatives Towards New Materials and Applications

- Evaluation of new materials for metal deposition systems
  - Achieve low resistance with thin wire
  - Excellent gap fill capabilities



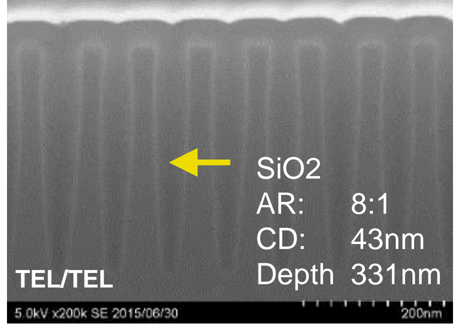


Film formation in processing

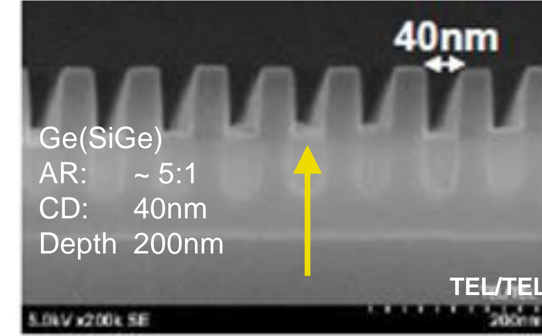


After formation

- Develop anisotropic deposition and selective deposition
  - Achieving gap fill and bottom up processes by using TEL's unique deposition technique



Gap fill



Bottom up

Expanding SAM through the development of new applications for miniaturization

Augmenting Production System

New building at Yamanashi (Fujii) Plant

- Construction start (scheduled): January 2019
- Completion (scheduled): April 2020
- Products: Single wafer deposition, gas chemical etch, and test systems

New building at Tohoku Plant

- Construction start (scheduled): October 2018
- Completion (scheduled):
  September 2019 (First phase)
  December 2020 (Second phase)
- Products: Thermal processing systems

Expand production system, flexibly respond to future growth in demand

Summary

- Deposition market continues to expand, especially in memory
- Expand our market share in the fields of ALD, single wafer CVD and thermal processing systems, by raising the competitiveness of our existing products and introducing new products
- Start construction of new factory buildings in FY2019, increase production capacity for sustainable growth

FPD Business Strategy

May 29, 2018

Tsuguhiko Matsuura
VP & GM, General Manager, FPD BU

FPD Medium-term Plan

FPD equipment market

($B)

Data based on IHS Markit, Technology Group, Display Supply Demand Equipment Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.

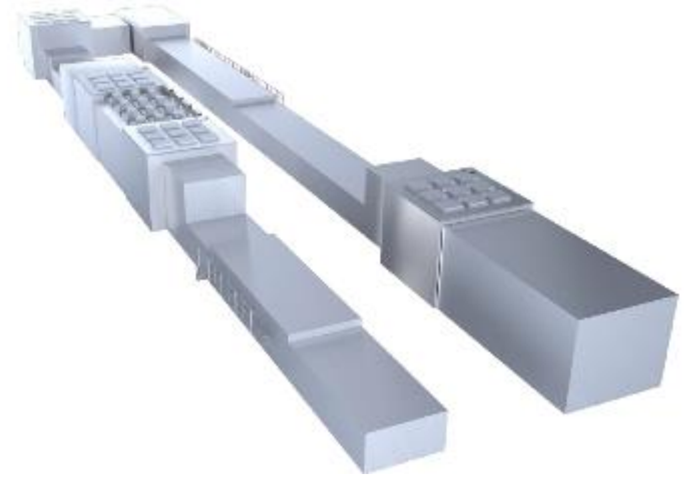
Sales and operating margin

(Billion yen)

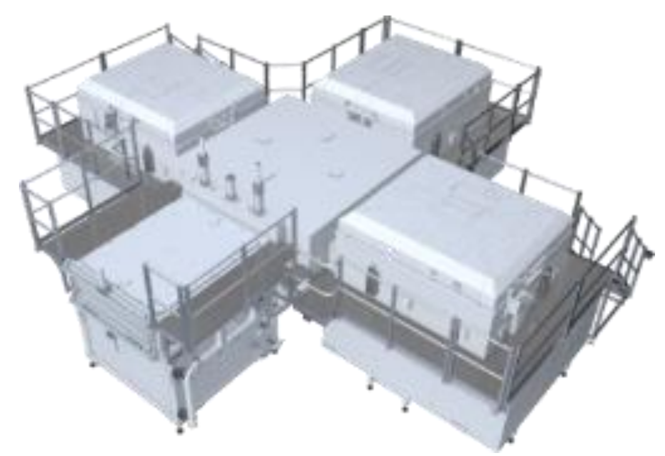
Progressing according to plan towards achieving 20% operating margin target in medium-term plan

Medium-term Plan Progress: Highlights

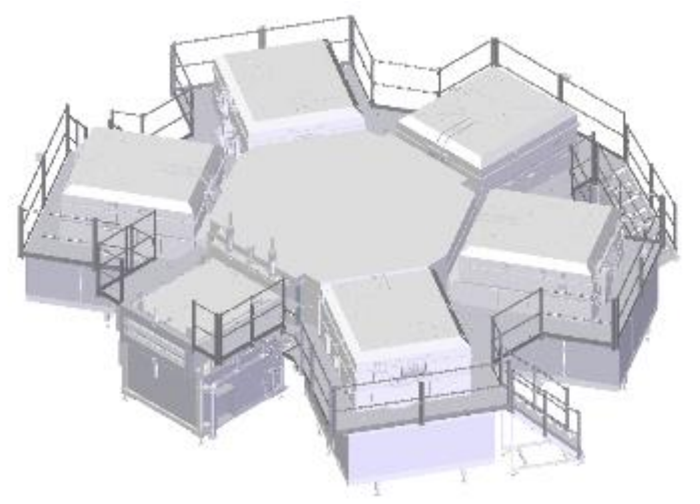
- Established our leading position in G10.5
- Introduced new Betelex™ platform etch system
- Expansion of PICP™* etch system going well



FPD coater/developer
Exceliner™



FPD plasma etch/ash system
Impressio™



FPD plasma etch/ash system
Betelex™

* PICP: Plasma source for producing extremely uniform high density plasma on substrate

Display Trends

Increasing screen size

OLED

Color filter
LCD
TFT
Backlight

Emissive layer
TFT

LCD --------> OLED

Increasing resolution

TV

FHD --> 4K --> 8K

Mobile, VR 300 ppi ------> 1000 ppi

Design flexibility

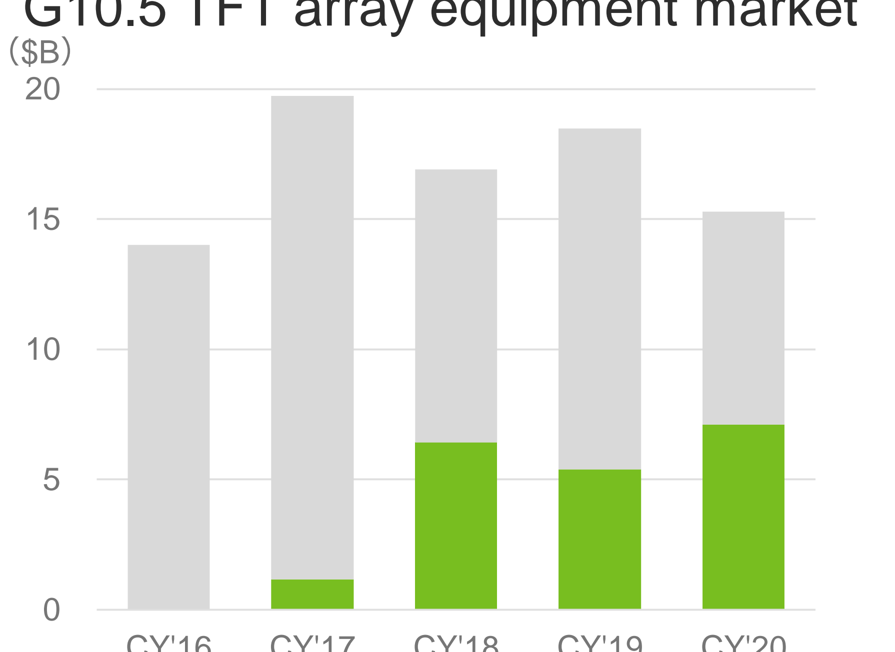
Flexible, edge bent, free format

Technological change in displays increasing business opportunities

Business Opportunity: G10.5 Equipment Market

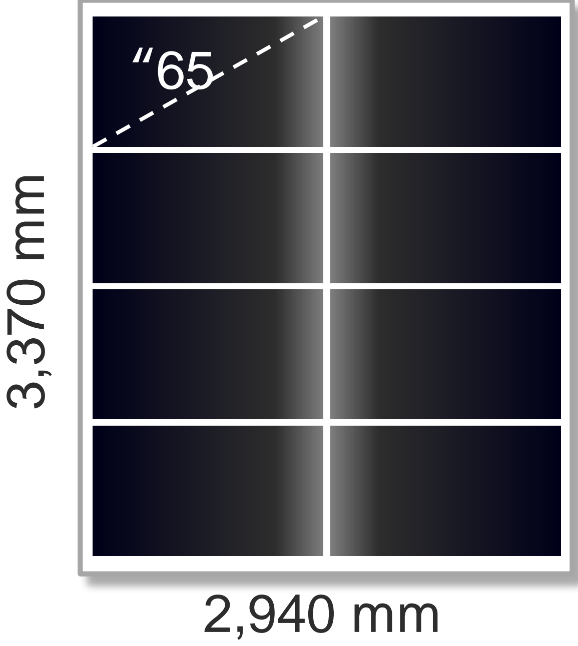
- Greater-than-expected growth in investment
- Maintain high market share through technological differentiation (large area plasma control, air floating coater)

G10.5 TFT array equipment market



Data based on IHS Markit, Technology Group, Display Supply Demand Equipment Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.

Eight 65 inch TV panel substrate possible



Increased sales far beyond market growth by meeting customers' technological needs

Business Opportunity: Metal Oxide/LTPS

TFT array	a-Si	Metal Oxide	LTPS
Representation of structure			
Application	LCD TV Monitor	OLED TV Tablet	Smartphone (LCD/OLED)
Number of masks	5	6-8	9-13
Dry etch processes	3 a-Si, SiNx	3 SiO, SiNx	~11 SiO, metal

Further new needs

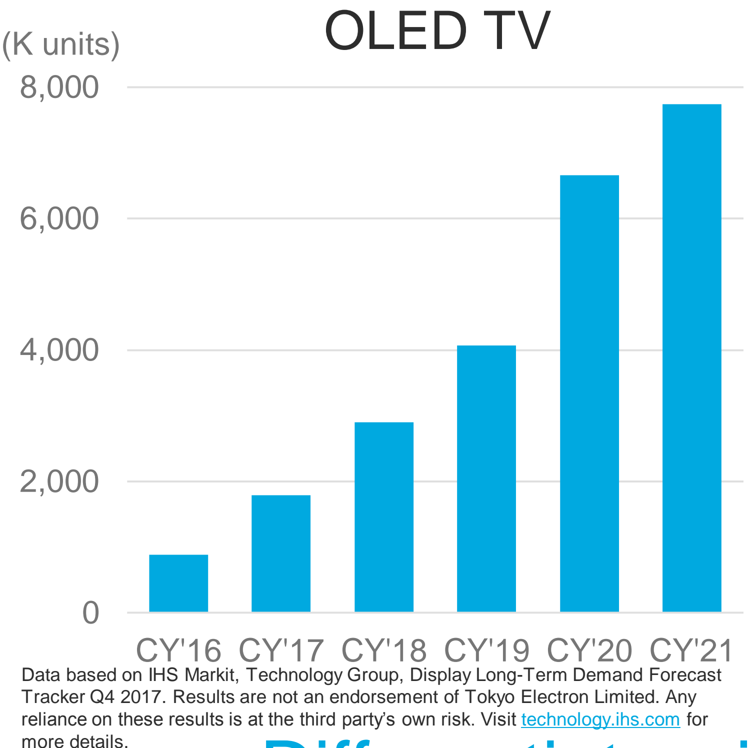
Flexible displays
+2 processes

OLED process
(G6 Half Size)
+3-4 processes

Number of etch processes increased as more advanced technology sought

Business Opportunity: Growth of OLED TV Market

- Material utilization significantly more efficient than current evaporation method
- Companies improving functionality of ink



Data based on IHS Markit, Technology Group, Display Long-Term Demand Forecast Tracker Q4 2017. Results are not an endorsement of Tokyo Electron Limited. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.

Inkjet printing system for manufacturing OLED planes
Elius™ 2500

Differentiate with inkjet printing system towards growth in the OLED TV market

Summary

- Increase share and profitability in growing market, business progressing according to plan
- New medium-term plan FY2021 target: sales ¥100.0B, operating margin over 20%
- For leading-edge production processes, focus on areas where we have technological superiority
  - High performance PICP™ etch system
  - Etch system and coater/developer for G10.5 substrate
  - Inkjet printing system for OLED TVs

TEL™
TOKYO ELECTRON