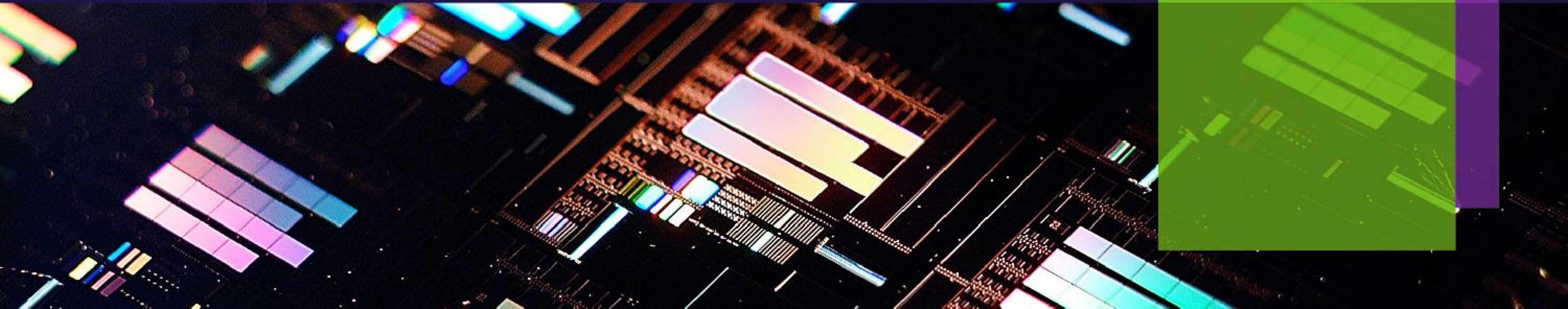
TOKYO ELECTRON

Medium-term Management Plan (abridged version)

July 12, 2022

SEMICON West 2022 IR Meeting



Forward Looking Statements

- Disclaimer regarding forward-looking statements
  Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, intellectual property-related risks, and impacts from COVID-19.

- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Exchange risk
  In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD production equipment are denominated in yen. Although some sales and expenses are denominated in foreign currencies, the impact of exchange rate fluctuations on profits is negligible.

FPD: Flat panel display

Medium-term Management Plan Briefing 2022 Program and Participants

- Presentation
  - The New Medium-term Management Plan — Toshiki Kawai
  - Technology trends and TEL™'s business opportunities — Akihisa Sekiguchi
  - SPE Business Strategy — Yoshinobu Mitano

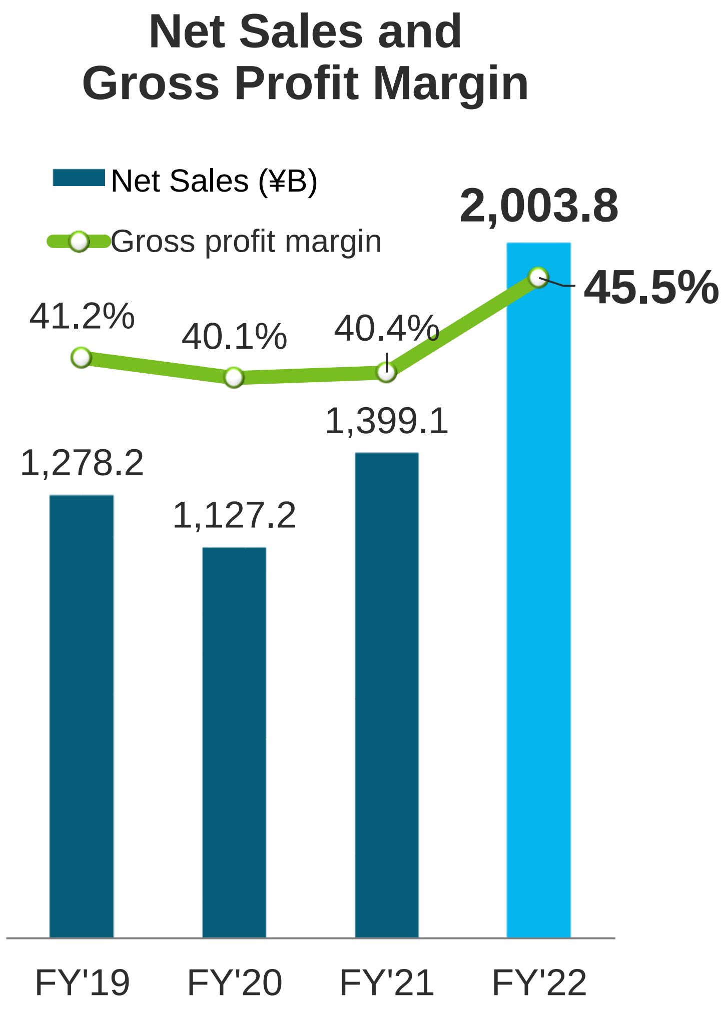
- Q&A Session

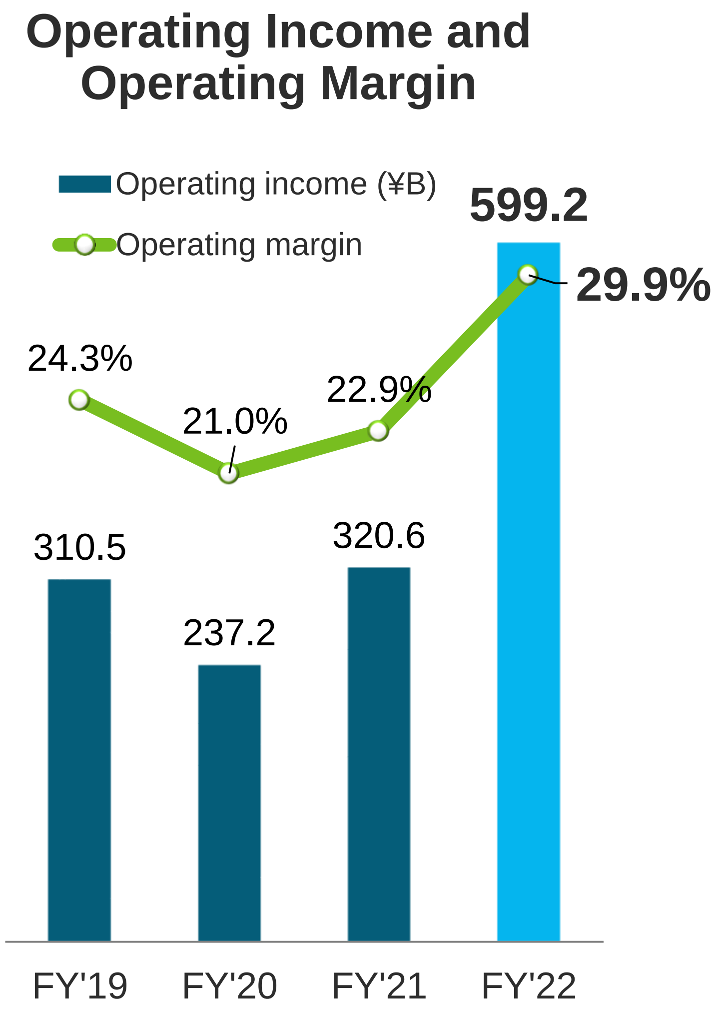
The New Medium-term Management Plan

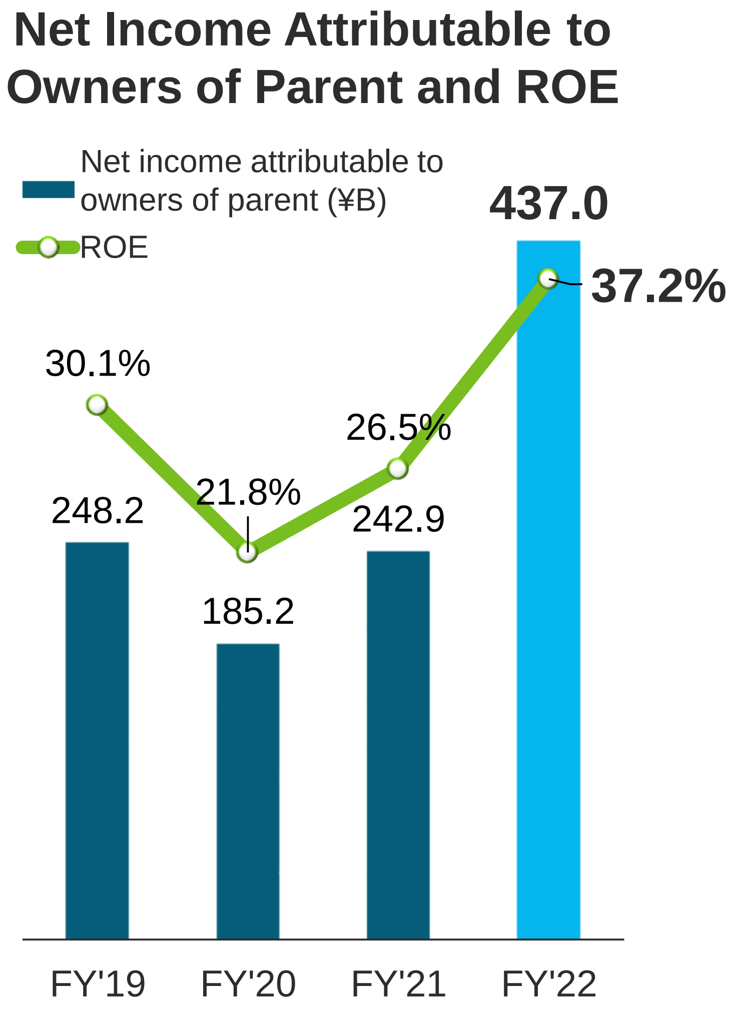
July 12, 2022

Toshiki Kawai
Representative Director, President & CEO

FY’22 Financial Highlights

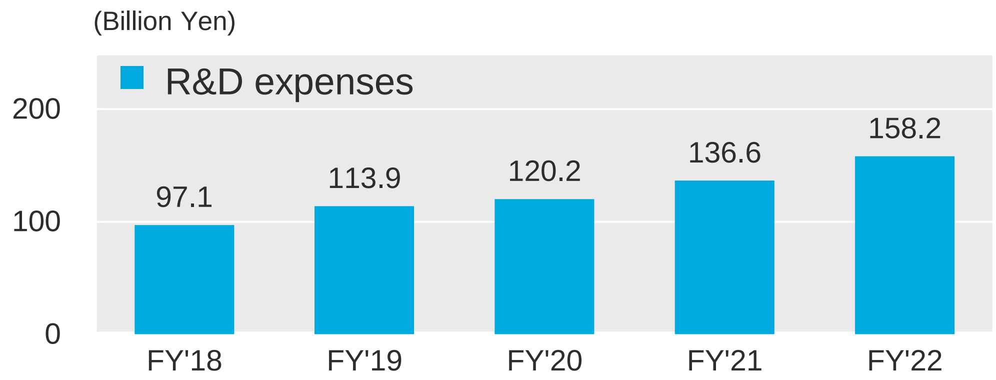


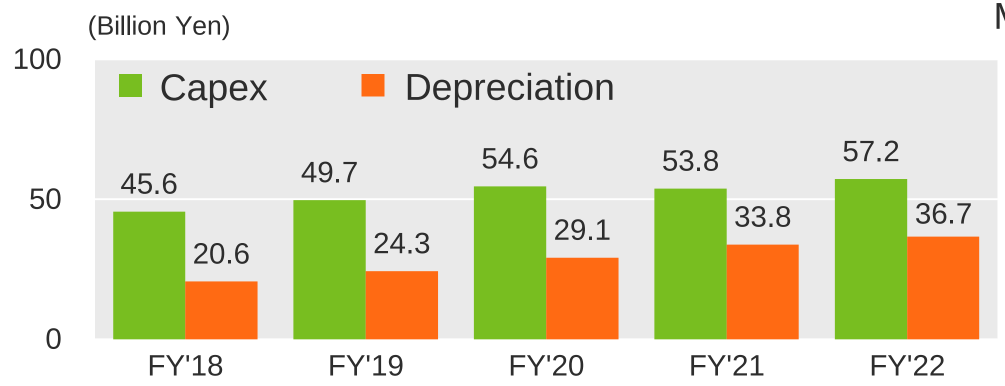




Net sales, gross profit margin, operating margin and ROE reached record high

Performance of Growth Investments Made Over the Past Five Years





Miyagi logistics building
(Began operation in 2018)

Production capacity doubled

Iwate production building
(Began operation in 2020)

Production capacity doubled

Yamanashi production building
(Began operation in 2020)

Production capacity 1.5 times

Miyagi No.2 development bldg.
(Began operation in 2018)

TEL Digital Design Square
(Began operation in 2020)

Miyagi Technology Innovation Center
(Began operation in 2021)

Invested on increases in production capacity, enhancement of development capabilities, advancement of DX, and partnerships with suppliers

Progress on the Medium-term Management Plan

Announced on May 2019

	Financial Model (by FY'24)		
Net sales	1.5T yen	1.7T yen	2T yen
OP margin	26.5%	28%	>30%
ROE	>30%		

FY'22 Actual
2T 3.8B yen
29.9%
37.2%

Reached our financial model 2 years ahead of schedule

Background of the Achievement of the Medium-term Management Plan Two Years Ahead of Schedule

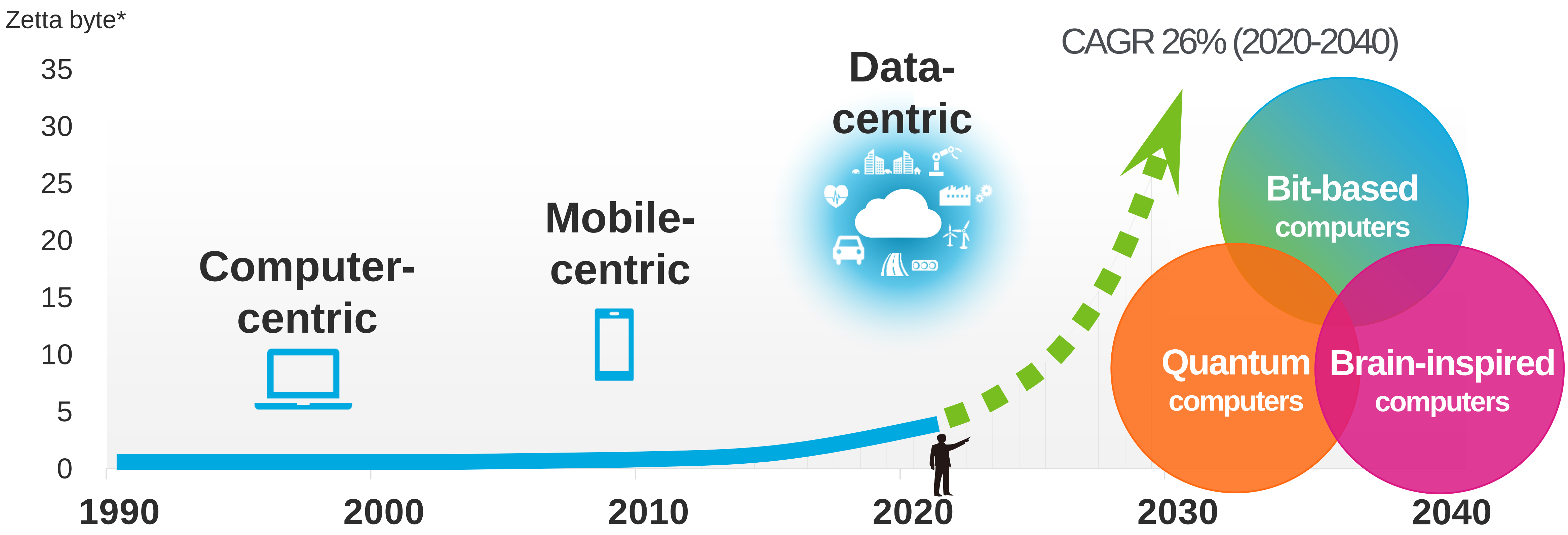
- Continued to invest in R&D even during the market adjustment period when sales declined
- Collaborated closely with many of technologically advanced suppliers located around our plants, created differentiated technology, and worked together to overcome disruptions in procurement and logistics
- TEL employees with a spirit of challenge responded to the changing environment amid the strict lockdown and travel restrictions imposed by COVID-19

The New Medium-term Management Plan

- Business Environment
- Overview of the New Medium-term Management Plan

Global Data Traffic

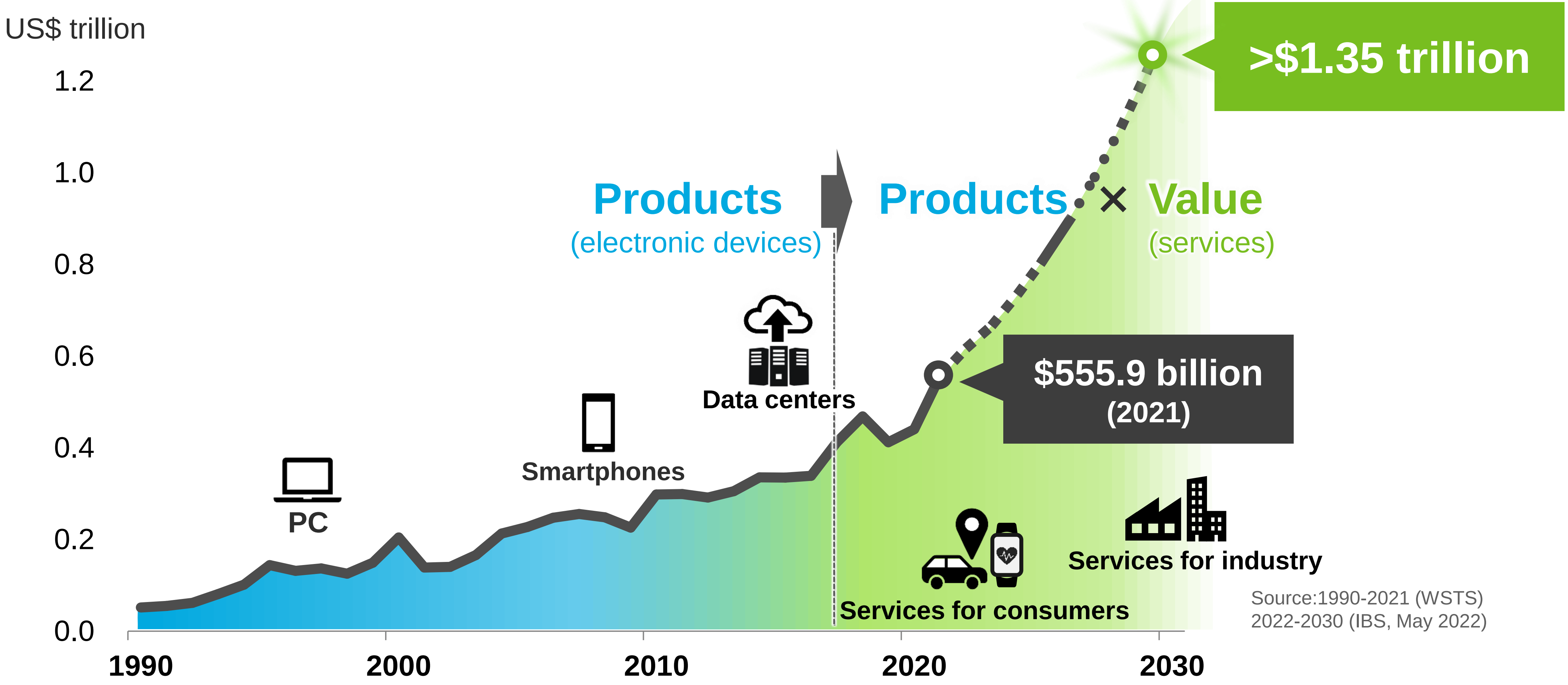
Data volume will increase **100x** in 20 years



Source : Omdia

The digitization of society has only just begun.
Computing evolves into the true big data era

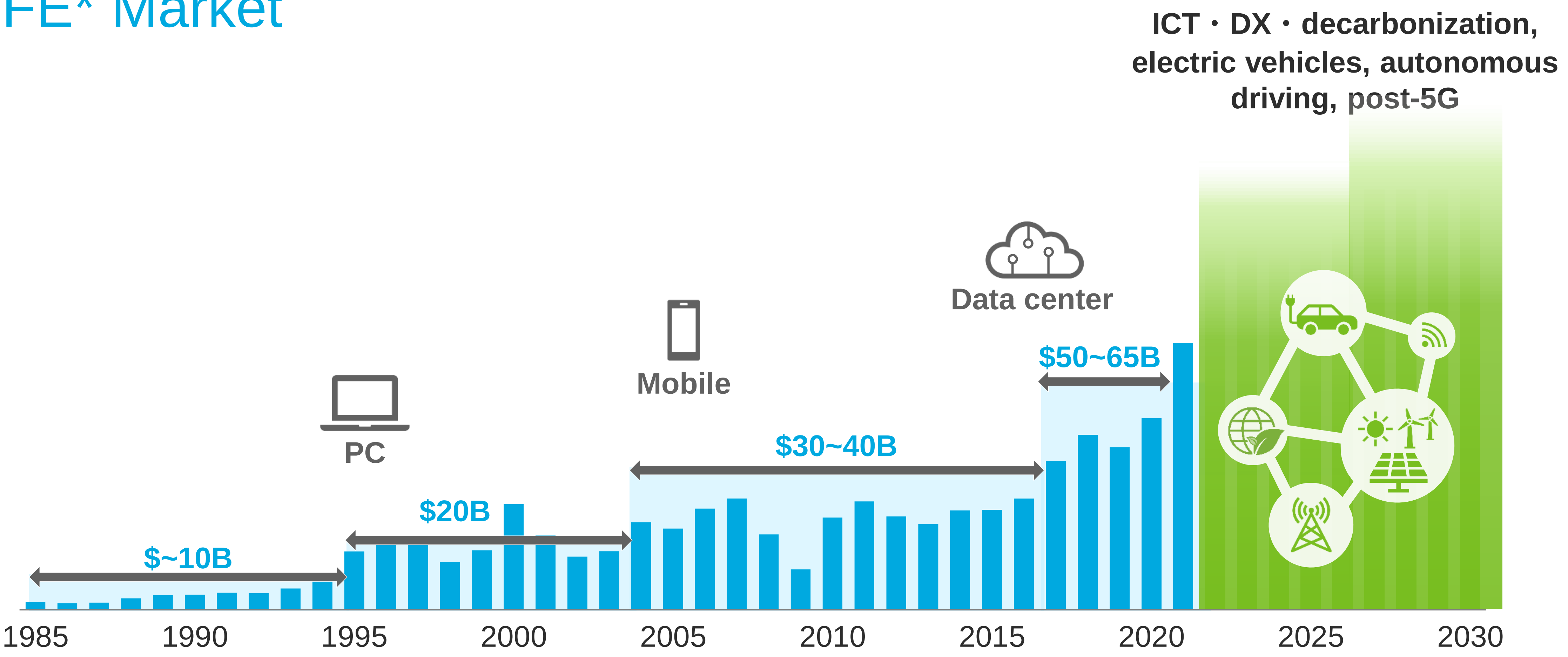
Outlook for the Semiconductor Market



Source:1990-2021 (WSTS)
2022-2030 (IBS, May 2022)

Growing to more than double by 2030

WFE* Market



Source：TechInsights Manufacturing Analysis Inc. (VLSI) (1985-2021)

WFE Market will grow further with progress of digitalization and evolution of semiconductors

*WFE (Wafer fab equipment): Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.

The New Medium-term Management Plan : Financial Targets

Financial Targets (by FY'27)	
Net sales	≥ 3 trillion yen
OP margin	≥ 35%
ROE	≥ 30%

Big Global Trends

“In order to build a strong and resilient society in which economic activities do not stop under any circumstances”

Pushing firmly ahead with the implementation of ICT*

Taking action to realize a carbon-free society

* ICT : Information and Communication Technology

Increasing Importance of Semiconductors

Taking Advantage of TEL’s Strengths

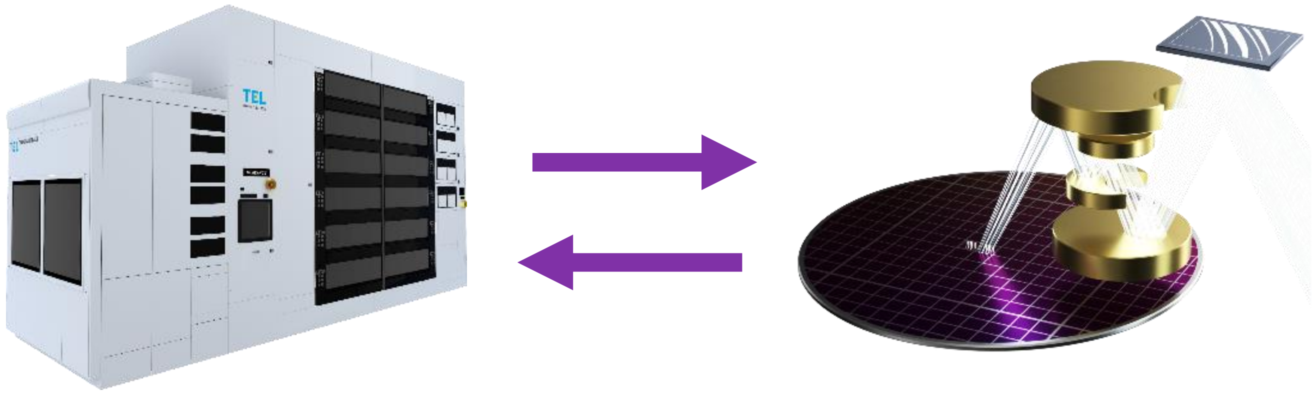
Only one

Deposition **Coater/developer** **Etching** **Cleaning**

Have products in 4 sequential processes

Taking Advantage of TEL’s Strengths

100%



Coater/developer EUV lithography

100% share of coater/developer for EUV lithography

EUV: Extreme Ultraviolet

Major products and market position*

#1	#2	#2	#1	#1	#1	#2	#1
							
Coater/ developer	Cleaning	Plasma etch	Gas chemical etch	Diffusion furnace	Batch deposition	Metal deposition	Prober

*TEL estimate

Products with the world's No.1 or No.2 market share

Taking Advantage of TEL's Strengths

No.1

Industry's largest install base

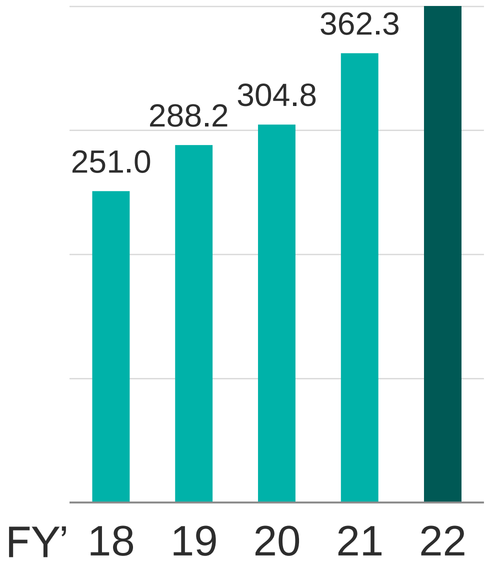
82,000 units

Annual increase by about

6,000 units

Field Solution Sales

455.9B yen



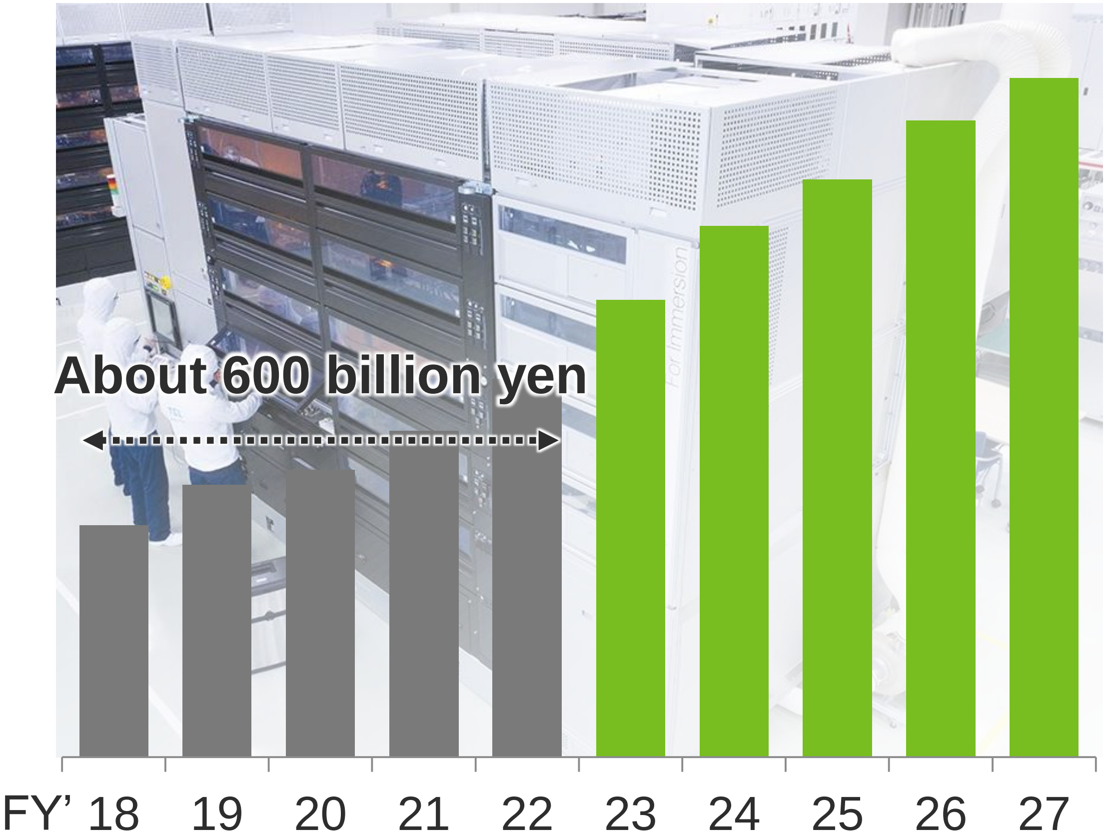
Equipment sold creates new business opportunities

Every leading-edge semiconductor in the world passes through our equipment

Profit is an important measure of value in our products and services

Further improving strengths

Continue to Invest Aggressively on R&D



More than 1 trillion yen planned for 5 years from FY'23

Continue active investment in growth to create high value-added next-generation products

FY60th

New Vision

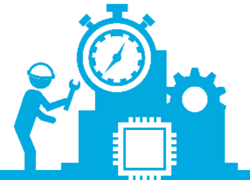
New Vision

A company filled with dreams and vitality that contributes to technological innovation in semiconductors

Tokyo Electron pursues technological innovation in semiconductors that supports the sustainable development of the world.

We aim for medium- to long-term profit expansion and continuous corporate value enhancement by utilizing our expertise to continuously create high value-added leading-edge equipment and technical services.

Our corporate growth is enabled by people, and our employees both create and fulfill company values. We work to realize this vision through engagement with our stakeholders.



Corporate Message

Technology Enabling Life

TSV : TEL’s Shared Value

CSV (Creating Shared Value)

The concept is to create social and economic value by leveraging corporate expertise to solve social issues, thereby enhancing corporate value and achieving sustainable growth.

TEL’s CSV

TSV

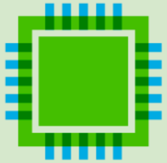
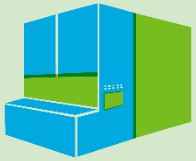
TEL’s Shared Value

Contributing to technological innovation in semiconductors

Approaches to Sustainability

E-COMPASS

Environmental Co-Creation by Material, Process and Subcomponent Solutions

Semiconductors	Production equipment	Business activities
Pursuing higher device performance and lower power consumption 	Achieving both high process performance and environmental performance of the equipment 	Reduction of CO_2 emissions in all business activities 

Promoting technological innovation of semiconductors and reducing environmental impact throughout the supply chain

Aiming for Sustainable Development of the World

Net Zero

Scope 1 & 2	**To be achieved by 2040**
Scope 3	**To be achieved by 2050**


Technology
Enabling
Life

Technology trends and TEL's business opportunities

July 12, 2022

Akihisa Sekiguchi, Ph.D.
Fellow, Corporate Innovation Division

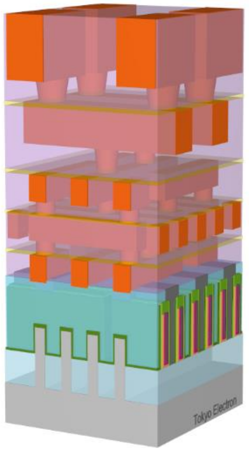
Overview

- Development Trends for Key Devices
- Technology Trends and Business Opportunities
  - Logic
  - DRAM
  - NAND
  - CMOS Image Sensor
- Summary

Development Trends for Key Devices

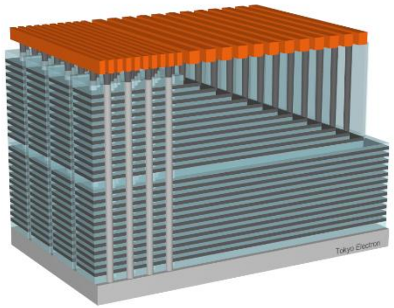
Semiconductor Devices: Direction of Development

Logic



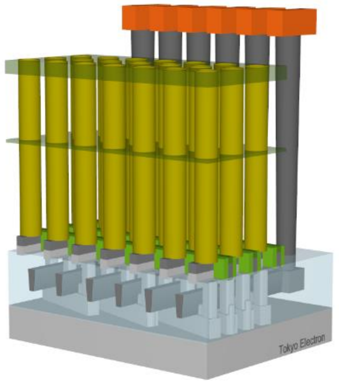
Through miniaturization with structural changes
- Lowered cost per transistor
- Lower power consumption
- Higher speed

NAND



Through high stacking
- Lower cost per bit

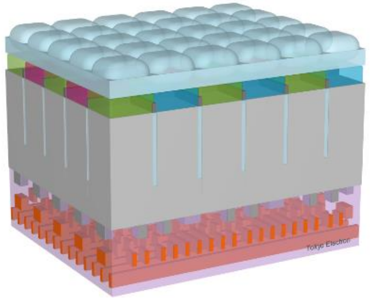
DRAM



Through miniaturization
- Lower cost per bit
- Lower power consumption
- Higher speed

Through new structures
- Lower cost per bit

CIS



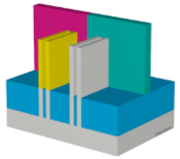
Through miniaturization
- Increased number of pixels
- Higher speed

Through new structures, new materials
- Greater image quality

Logic Trends and Business Opportunities

Advances in Smartphone CPUs

Product Year	2014	2020
Tech. Node	20nm	5nm
Transistor	Last Gen. Planar	4^{th} Gen. FinFET
Adv. Litho	ArFi	EUV
Die Size	$89mm^2$	$88mm^2$
Transistor#	2B	11.8B
CPU Cores#	2	6
GPU Cores#	4	4
NPU Cores#	N/A	16
L2/L3 Cache	5MB	28MB



×5.9

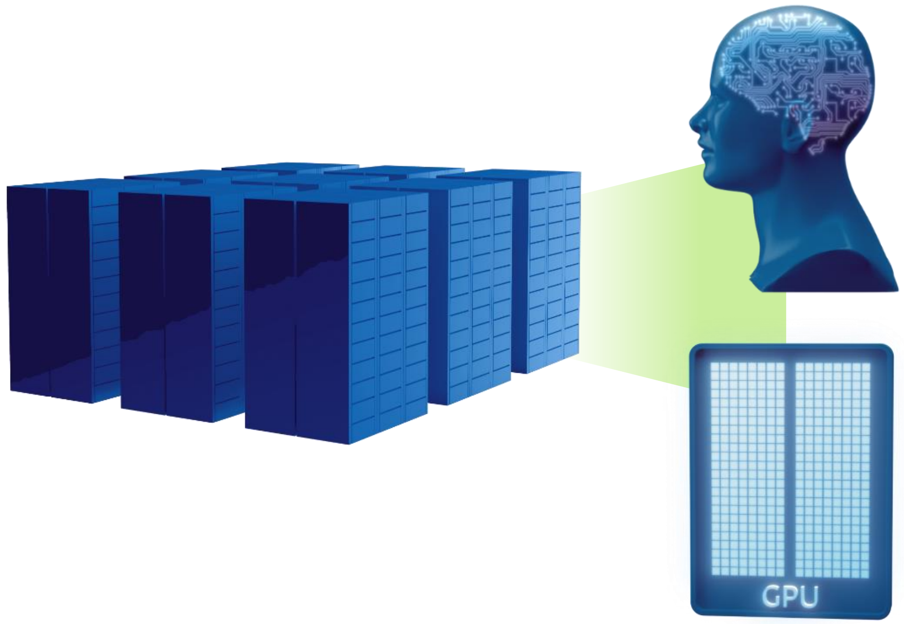
New architecture
Many cores
New function

×5.6

Source: Wikipedia https://en.wikipedia.org/wiki/Apple_A14 https://en.wikipedia.org/wiki/Apple_A8 https://en.wikipedia.org/wiki/Ampere_(microarchitecture)

With advances in transistor fabrication, materials and lithography, can improve integration by increasing transistor numbers, expanding functions, etc.

Advances in GPU (Operational Accelerator)



Product Year	2016	2020
Tech. Node	16nm	7nm
Transistor	1st Gen. FinFET+	3rd Gen. FinFET
Adv. Litho	ArFi	ArFi
Die Size	610mm^2	826mm^2
Transistor#	15.3B	54.2B
INT32/FP32 Mixed Cores#	3584	6912
FP64 Cores#	1792	3456
L1/L2 Cache	5.440MB	61.696MB

×3.5

New architecture
Many cores
New function

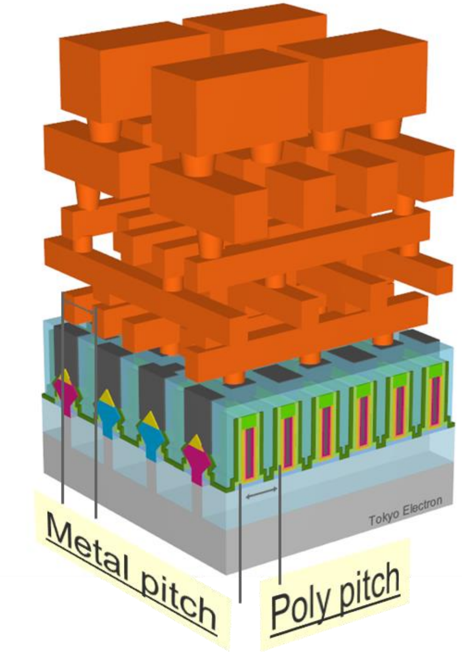
×11.3

Source: Wikipedia https://en.wikipedia.org/wiki/Apple_A14 https://en.wikipedia.org/wiki/Apple_A8 https://en.wikipedia.org/wiki/Ampere_(microarchitecture）

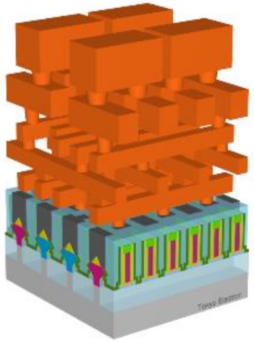
Number of transistors increasing in HPC too, visible trend toward expansion of functions
Higher integration also sought

Advances in Logic Integration Density

Pitch shrink



Shrink



Key enablers

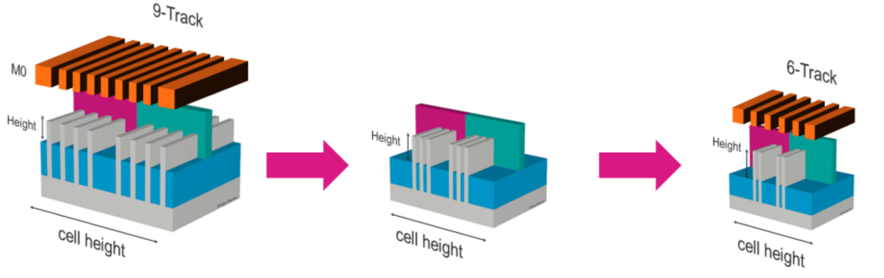
- EUV patterning
- Small area gap filling
- High selective etch
- Pattern collapse free drying

Further advances in lithography, etch, thin film deposition and cleaning technologies needed for miniaturization

Advances in Logic Integration Density

Design Technology Co-optimization: DTCO

① Cell height scaling: Fin depopulation, Metal track# reduction

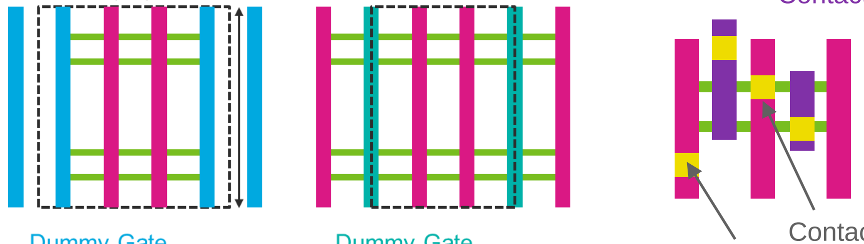


1st gen FinFET　　2nd gen FinFET　　3rd gen FinFET

Key enablers

- Narrow, straight etch
- Loading free recess etch
- Fin capping to prevent oxidation
- Low resistance silicide, metal

② Cell width scaling: Single Diffusion Break, Contact Over Active Gate etc.



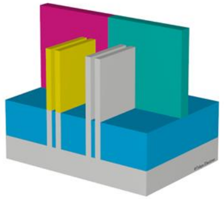
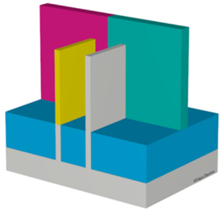
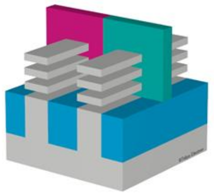
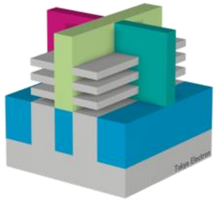
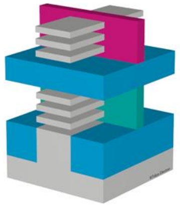
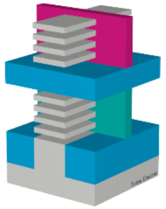
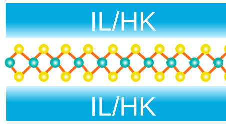
Key enablers

- Small hole, trench etch
- Low stress gap filling
- Multi-color films for etch
- High selective etch

Further advances in process technology for DTCO sought

Logic Technology Roadmap: Generic

Source: TEL estimates

Year of HVM (20k/month)	2020	2022	2024	2026	2028	2030	2032
Node	N5	N3	N2	N1.4	N1	N0.7	N0.5
Device	2 Fin 	2~1 Fin 	GAA NS 	Forksheet 	CFET 	2nd Gen. CFET 	 2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.
Poly pitch (PP)	51	45	42	39	36	33	30
Min. MP [nm]	28	22	20	18	16	12	12
Cell height (CH)	210 (2Fin)	162 (2Fin)	120 (NS)	90 (NS)	64 (CFET)	48 (CFET)	36 (CFET)
Density (a.u.) PP x CH x DTCO*	1	1.69 (vs. N5)	1.66 (vs. N3)	1.65 (vs. N2)	1.75 (vs. N1.4)	1.67 (vs. N1.0)	1.69 (vs. N0.7)
Scaling booster	EUV High μ channel	Mix cell	Backside PDN	High NA EUV Subtractive Ru	4-Track cell	Hetero channel New alloy	2D material

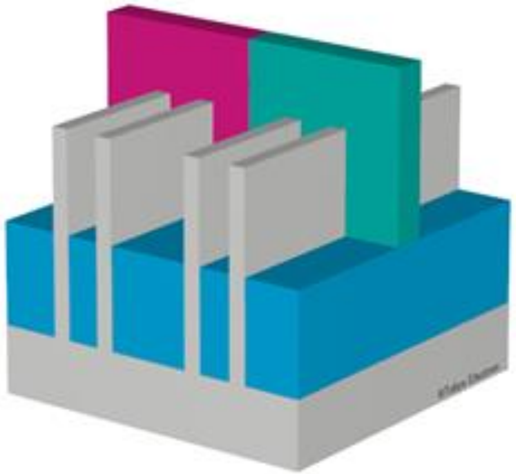
*Design Technology Co-Optimization:
Assume new knob will be created in each node for 1.15X

1.6-1.8x increase in logic density along with pitch scaling, DTCO and scaling booster

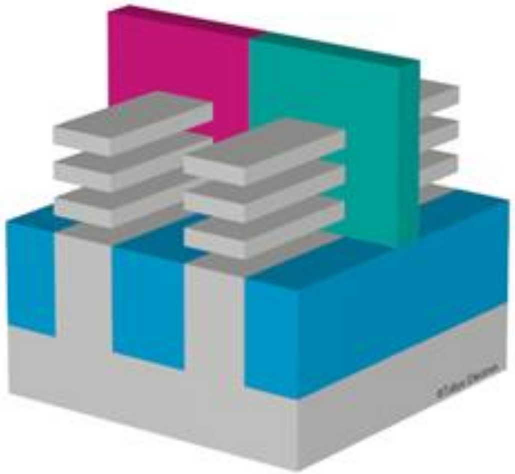
GAA Nanosheet Device (Gate All Around Nanosheet)

$$L_{g,min} \geq \beta(T_{ch}T_{ox}\varepsilon_{ch}/\varepsilon_{ox})^{1/2}$$

$L_{g,min}$: Minimum gate length with good device electrostatics
β : Constant > 2.5
T_{ch} : Channel thickness
T_{ox} : Gate oxide thickness
ε_{ch} : Dielectric constant of channel
ε_{ox} : Dielectric constant of gate oxide



Lay down



FinFET
Patterning defined Fin width: 3σ 1.1nm*

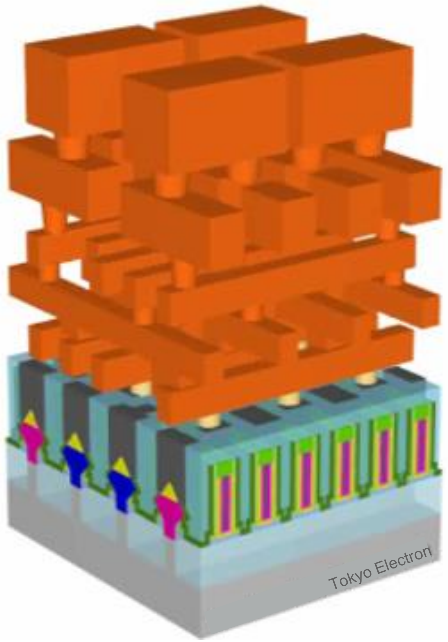
Nanosheet
Si EPI thickness defined sheet thickness: 3σ 0.4nm*

*Source: SC Song (Qualcomm) et al. VLSI 2019

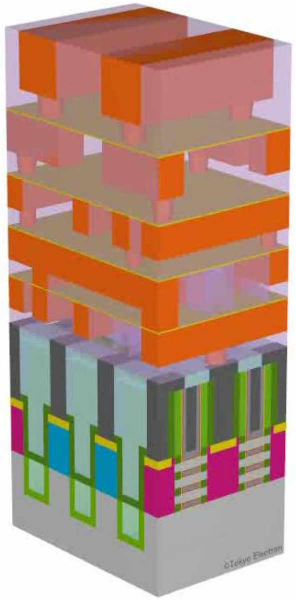
Improved controllability of channel width by nanosheet structure, increased channel width through stacking → Low leak, high on current

GAA Device Process Flow

FinFET



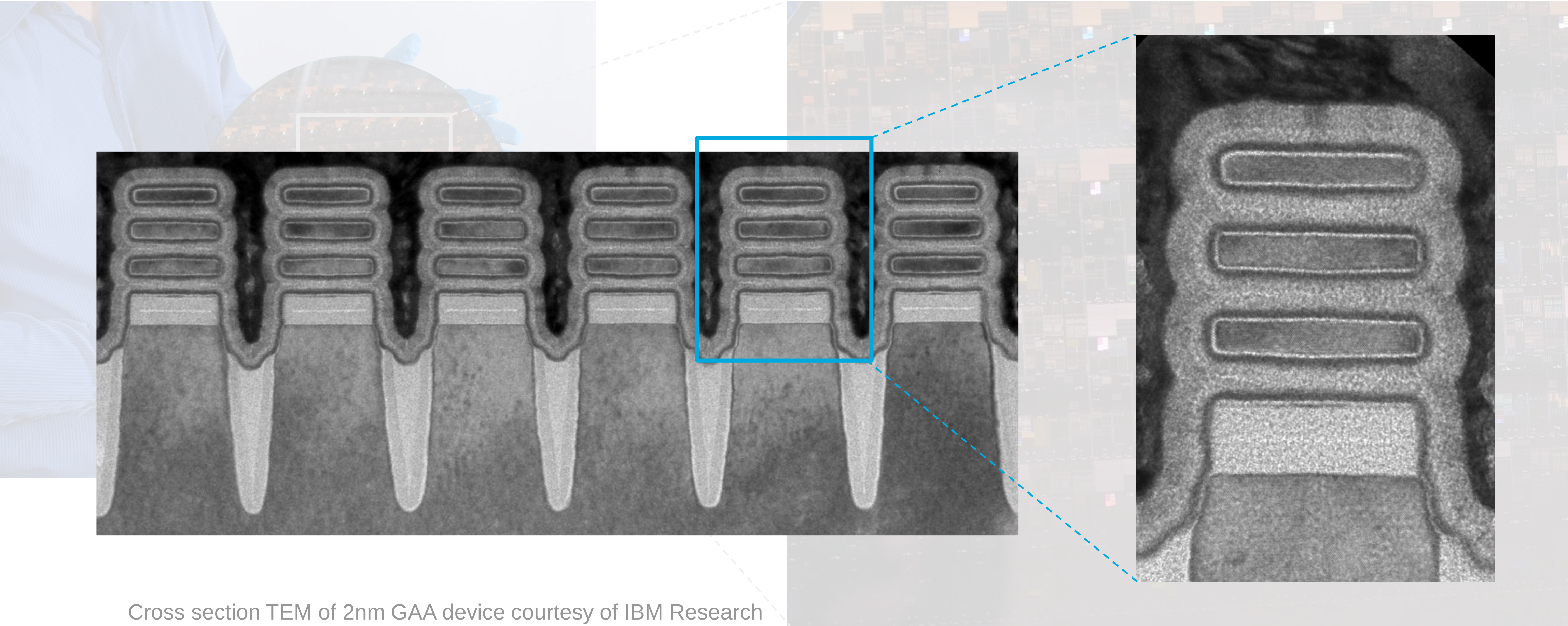
GAA FET



Source: TEL

TEL's wafer fab equipment is essential for creating complex GAA structures

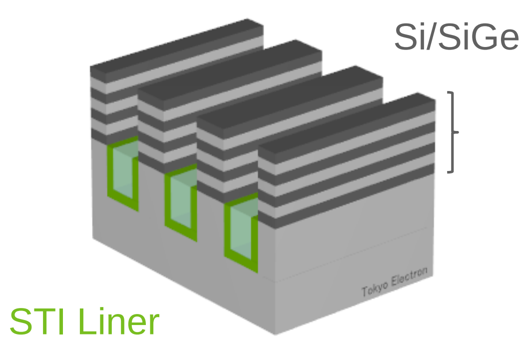
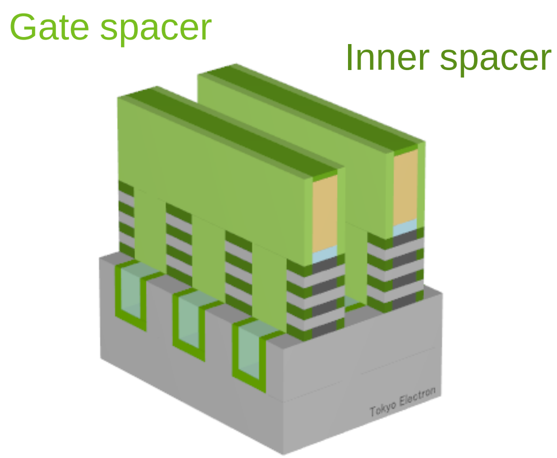
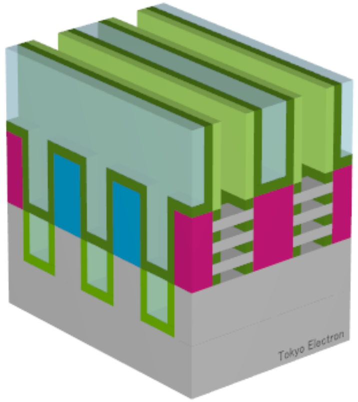
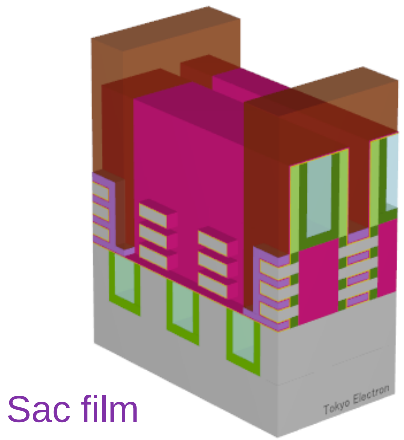
2 nm GAA Technology



Cross section TEM of 2nm GAA device courtesy of IBM Research

TEL's wafer fab equipment is essential for creating complex GAA structures

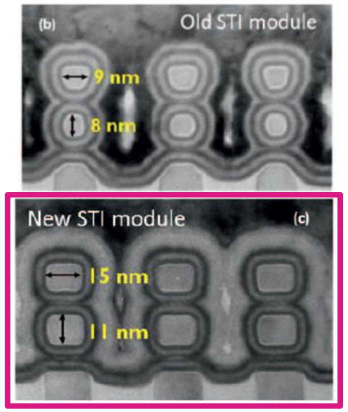
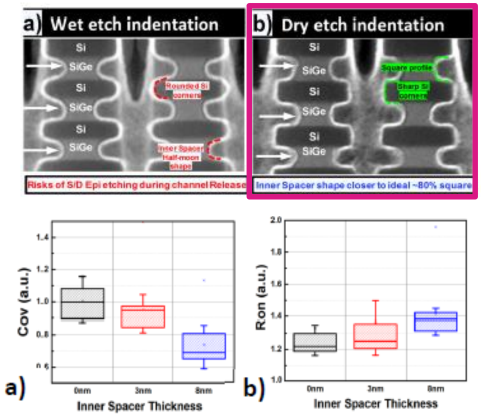
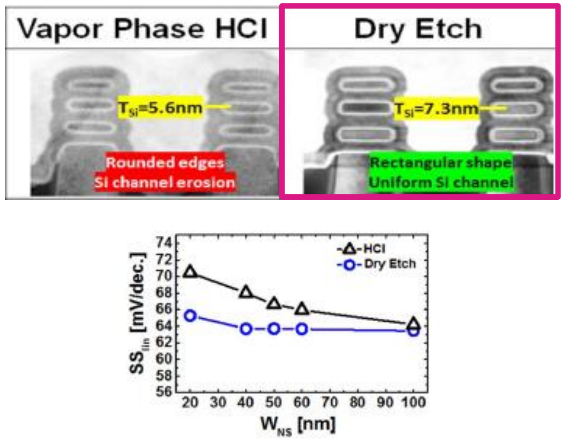
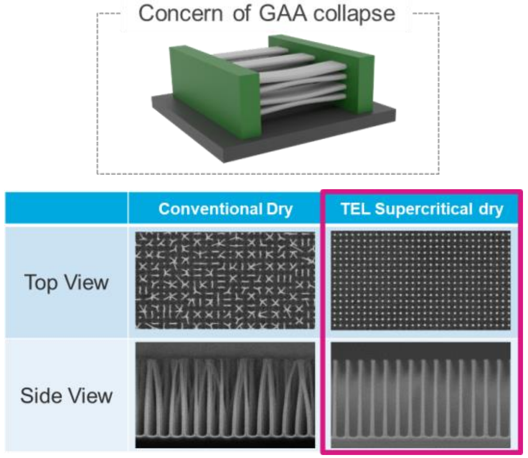
GAA Related Process Modules

Mold stack & Etch	Inner spacer	Nanosheet release	Replacement gate
			
• SiGe/Si: Defect free, Uniform EPI • Trench etch: Vertical profile • STI Liner: Prevent oxidation • STI OX: Low temp. • STI recess: Loading less	• Fin recess: Vertical profile • Indent etch: Loading less • Inner spacer dep: Low-k (k<5) • Inner spacer etch: High selective	• Full channel etch: High selective	• Reliability Si etch: High selective • Advanced drying: Collapse free • Sac film: Conformal • WFM/Dipole film: Conformal • WFM/Dipole etch: High selective

Source: TEL

Offering new solutions for critical modules in nanosheet devices

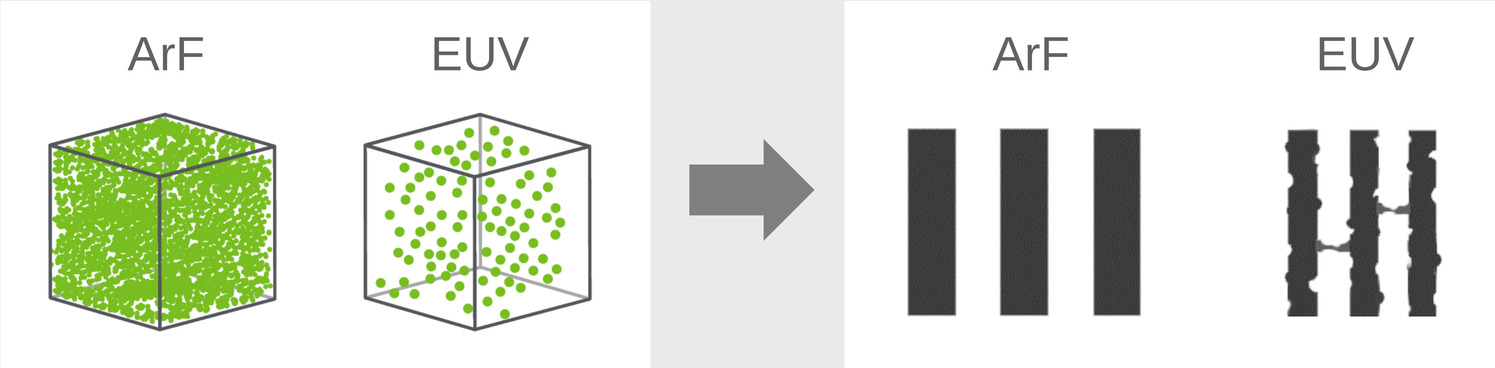
GAA Related Process Modules

Mold stack & Etch	Inner spacer	Nanosheet release	Replacement gate
 R. Ritzenthaler (imec) et al., iedm 2018	 N. Loubet (IBM) et al., iedm 2019	 N. Loubet (IBM) et al., iedm 2019	 Source: TEL
• SiGe/Si: Defect free, Uniform EPI • Trench etch: Vertical profile • STI Liner: Prevent oxidation • STI OX: Low temp. • STI recess: Loading less	• Fin recess: Vertical profile • Indent etch: Loading less • Inner spacer dep: Low-k (k<5) • Inner spacer etch: High selective	• Full channel etch: High selective	• Reliability Si etch: High selective • Advanced drying: Collapse free • Sac film: Conformal • WFM/Dipole film: Conformal • WFM/Dipole etch: High selective

Key points are preventing oxidation of Si/SiGe trench, high selectivity and precisely controllable SiGe etch, and preventing pattern collapse

Miniaturization: EUV Lithography Technology Challenges

Stochastic noise

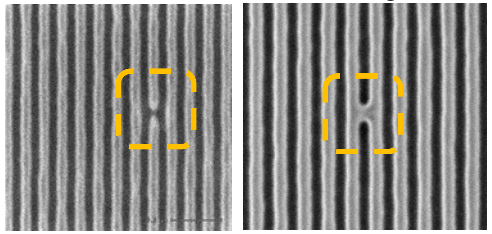


- The number of EUV photons is only **1/14** compared to ArF at the same dose.
- Photon absorption of EUV resist is lower than that of ArF resist.
- These cause large edge roughness, resulting in one of the sources of pattern defects.

Performance

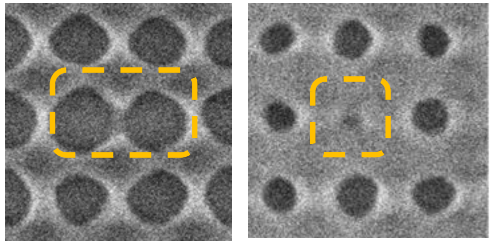
Line : LER, Pinching, Bridge

Pinching Bridge



Hole : L-CDU, Kissing, Missing

Kissing Missing

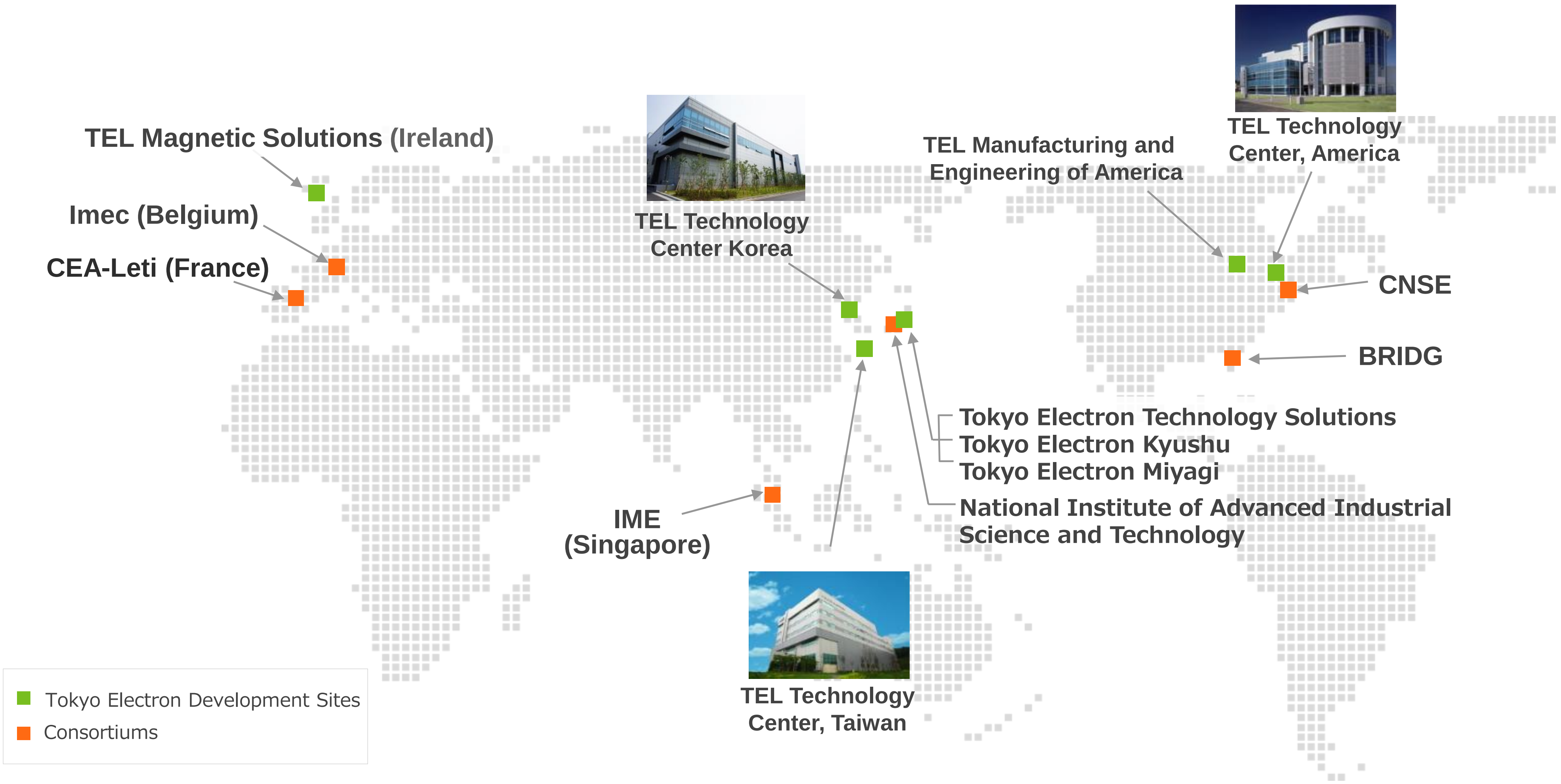


Source: S. Morikita, et al., Tokyo Electron Miyagi (DPS2018)

Resist stack and etching co-optimization necessary for realizing high productivity, precise control and low defects

Global Development Facilities

(As of June 1, 2021)

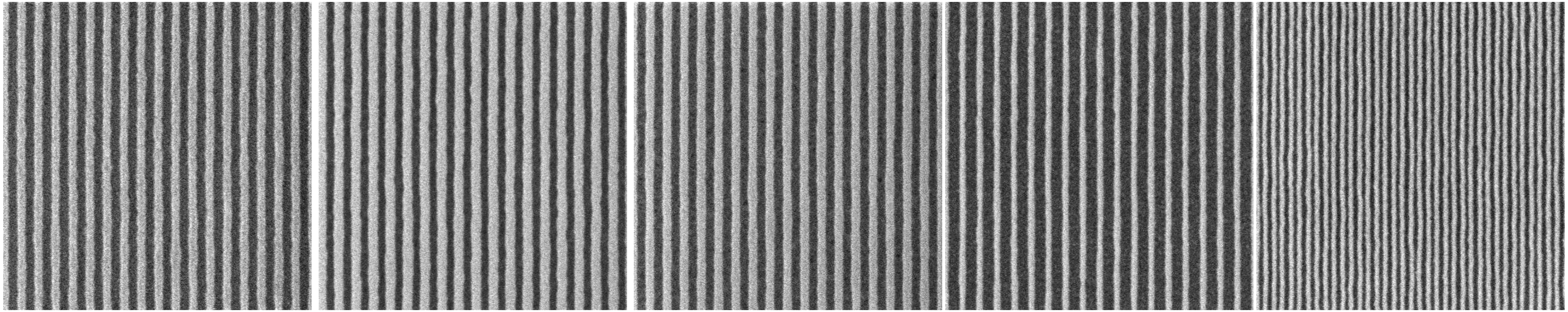


15 nm Pitch L/S Fabrication Using EUV SADP

Litho Pitch: 30nm
CDSEM CG6300
512*512/250k

Demonstrated on TEL tools

Lithography	Trilayer + Plasma Treatment	Tone Inversion	Mandrel	SEMP



Lithography	Trilayer + Plasma Treatment	Tone Inversion	Mandrel	SEMP
CD: 14.7nm	**LER: 2.0nm**	CD: 15.6nm	CD: 10.6nm	CD: 7.7nm
LER: 2.25nm	CD: 16.1nm	**LER: 1.89nm**	**LER: 1.71nm**	**LER: 1.57nm**

-11%

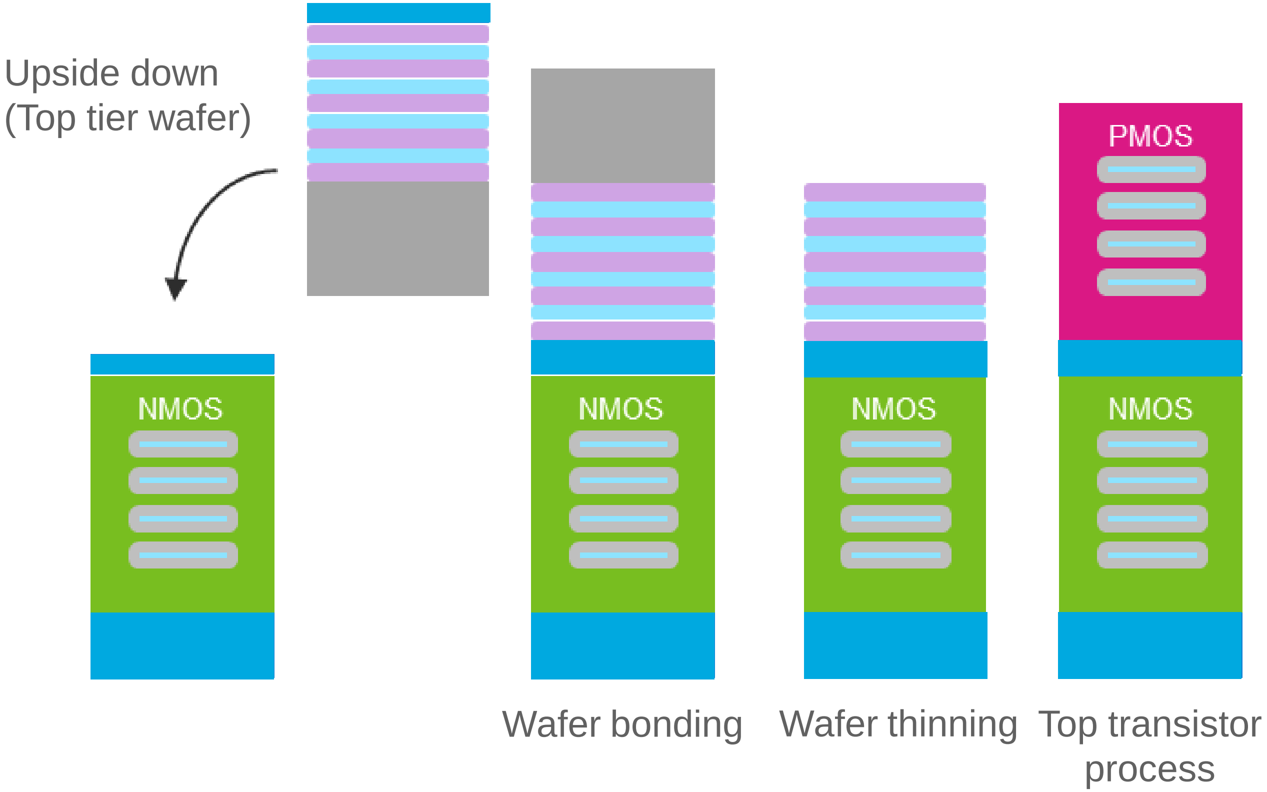
-24%

-30%

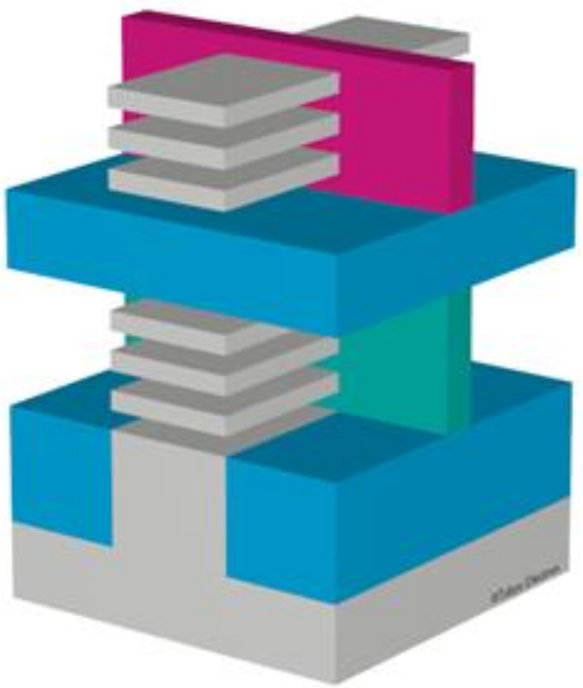
Source: Eric Liu et al., TEL Technology Center, America SPIE 2021 Advance Lithography

Achieve industry-leading 15 nm pitch line and space pattern

Back End: Wafer Bonding and Thinning Technology for CFET



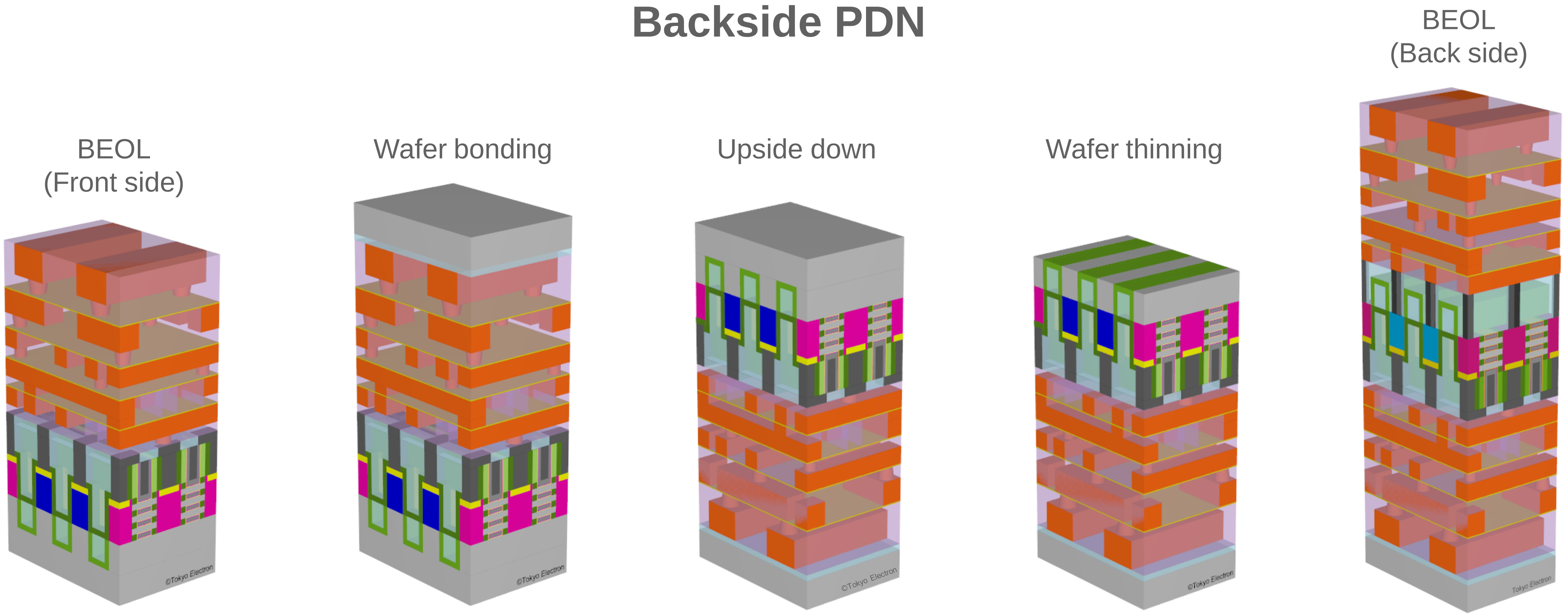
CFET



Low distortion wafer-to-wafer bonding technology and substrate film thinning technology are necessary for scaling booster technology

Back End: Wafer Bonding and Thinning Technology for BSPDN

Backside PDN



Low distortion wafer-to-wafer bonding technology and substrate film thinning technology are necessary for scaling booster technology

Wafer Bonding System

- Synapse™ Si
  - Integrate high high-productivity platform cultivated in the front-end process with plasma, cleaning and high-accuracy bonding modules
  - high productivity (uptime ≧ 90%)
    - alignment accuracy 3σ ≦ 50nm

High productivity and stable operation are realized at mass production fabs
Contribute to our customers to realize the future of "3D integration"

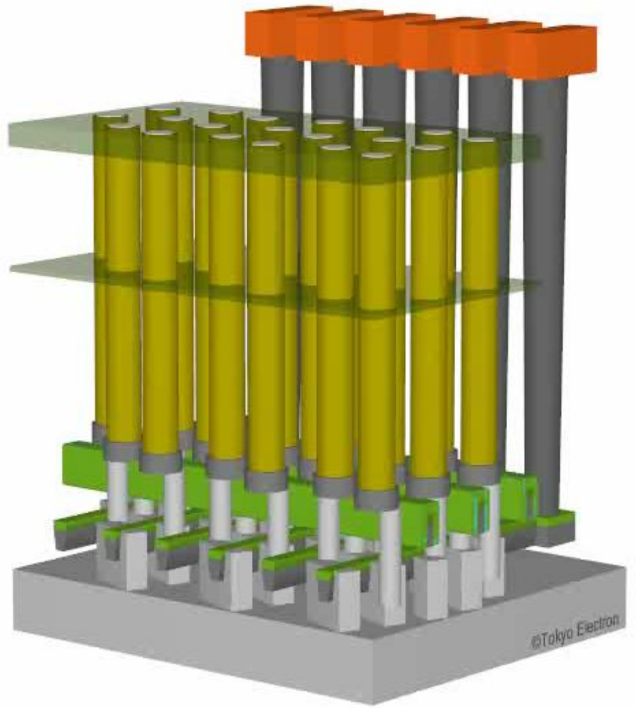
Laser Trimming System

- Ulucus™ L (New release)
  - Edge trimming on bonded wafer
  - Latest platform utilizing super clean technology from the front-end process, with the integration of laser control technology

Laser technology realizes high accuracy and quality trimming processes, and environment-friendly capability through the reduction of DIW usage

DRAM Trends and Business Opportunities

DRAM Structure and Process Flows



Source: TEL

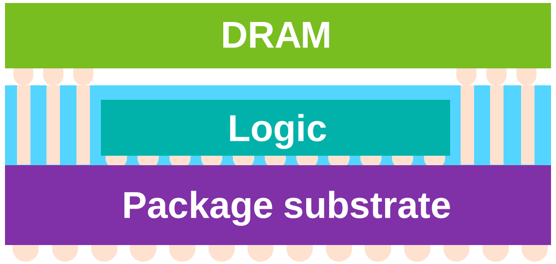
High aspect ratio structure is fabricated with sophisticated patterning technology

Advances in DRAM for Smartphones

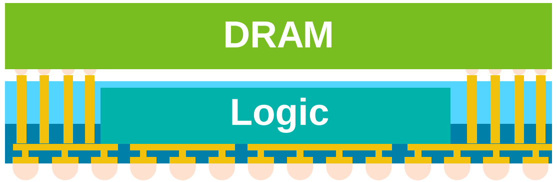
Product Year	2014	2020
Tech. Node	25nm	1ynm
DDR	LPDDR3	LPDDR4X
Data Rate	1.333Gbpps	4.266Gbpps
Capacity	1GB (4Gb ×2)	4GB or 6GB (8Gb or 12Gb×4)

×4 or 6

Source: Wikipedia https://en.wikipedia.org/wiki/Apple_A14 https://en.wikipedia.org/wiki/Apple_A8 https://en.wikipedia.org/wiki/Ampere_(microarchitecture)



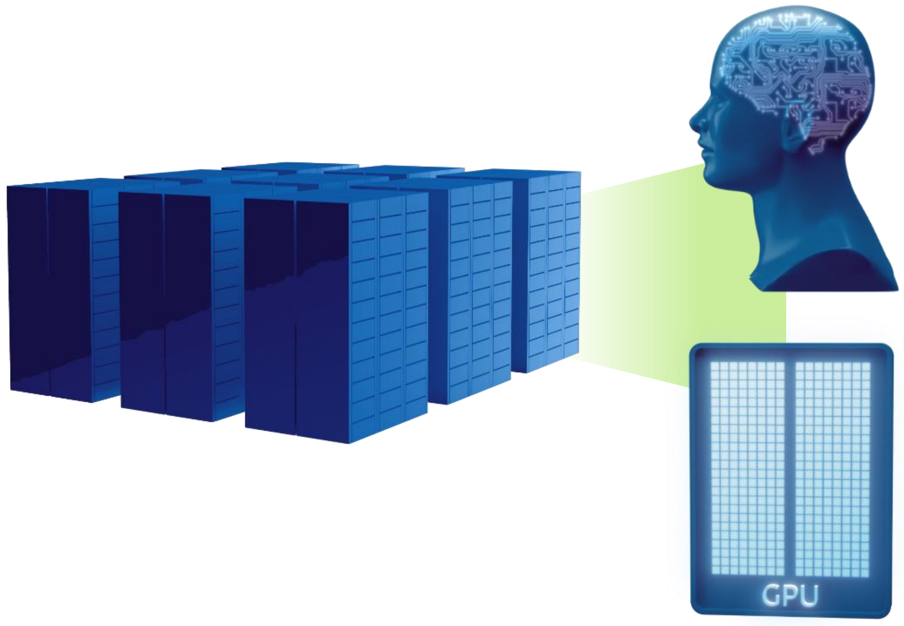
Flip Chip Package on Package



Integrated Fan-Out

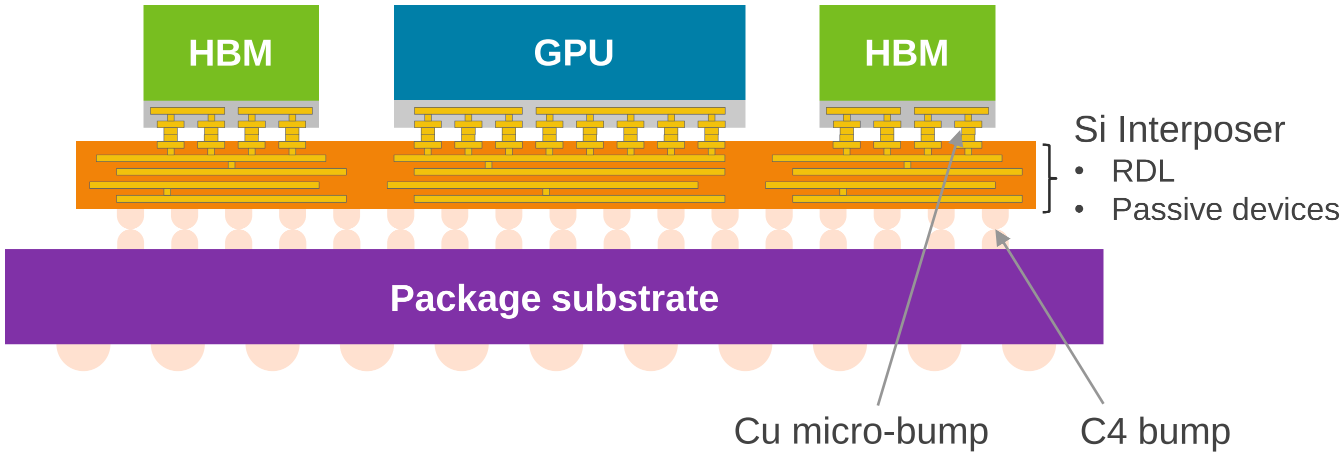
With the increase in data handling volumes, packaging has advanced with expanded capacity, accelerated processing and further integration

GPU (Operational Accelerator) and HBM DRAM



Product Year	2016	2020
Capacity	16GB HBM2 ×5 →	80GB HBM2e
	(HBM2×4)	(HBM2e×6)

Source: Wikipedia https://en.wikipedia.org/wiki/Apple_A14 https://en.wikipedia.org/wiki/Apple_A8 https://en.wikipedia.org/wiki/Ampere_(microarchitecture)



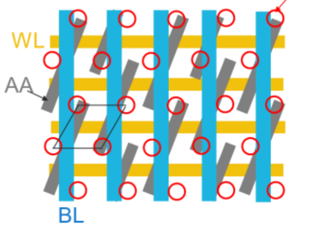
Data volumes are also increasing in HPC, driving packaging advances with increased integration, higher capacity and faster processing

DRAM Technology Roadmap

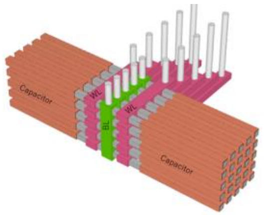
Source: TEL estimates

Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027~28	2029~30
F* [nm]	16	15~14		13~12	12~11		≦10	<10	
Pillar cap. A.R.	>40	>45		>50	>55		>60		

Cell / Peri. layout
- $6F^2$
- 3D



*Feature size: STI hp along WL = STI hp / COS(21º)

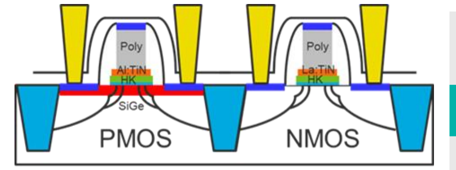


M. Popovici (imec) et al. IEDM 2018
Schematic by TEL

Patterning
- 193i SAQP, DP (+ EUV)

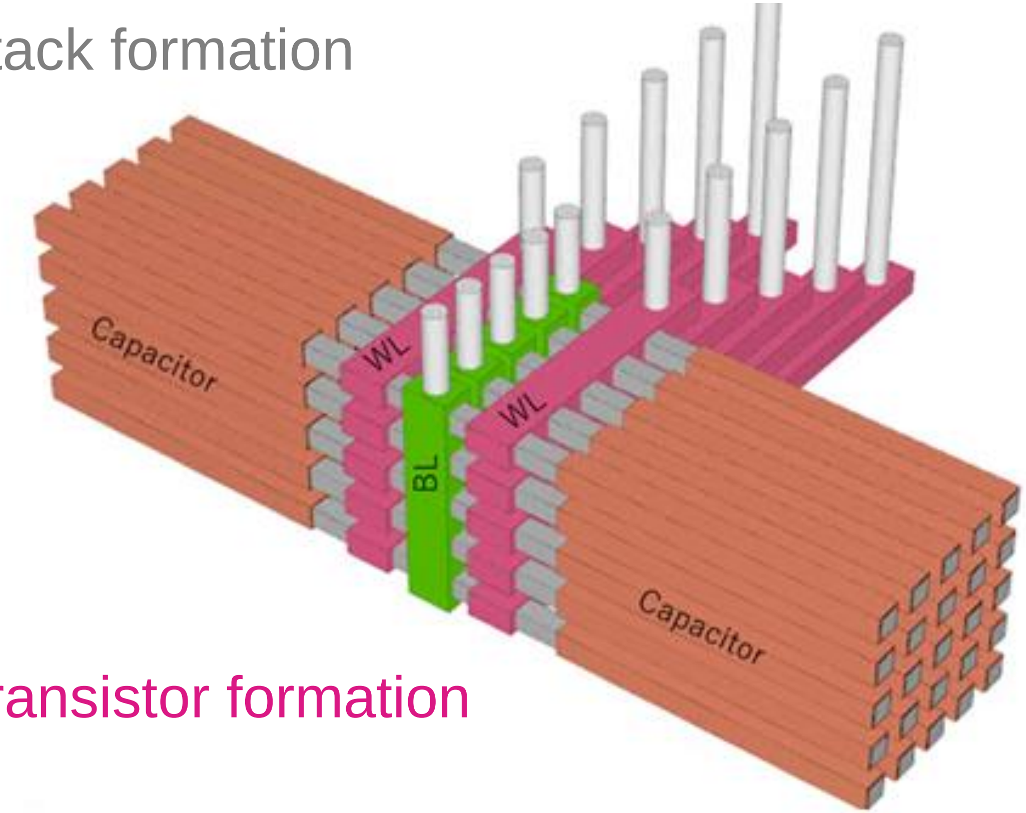
Capacitor
- ZAZ CIP
- Alternative: STO etc.

Peri. CMOS
- Poly SiON
- High-k Metal Gate
- FinFET



Key Modules in 3D DRAM

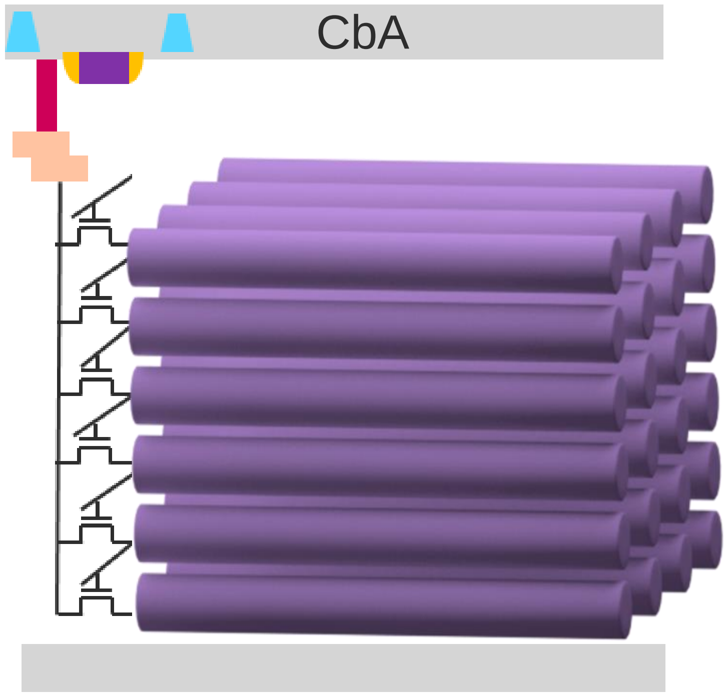
Stack formation



Cell Transistor formation

Capacitor formation

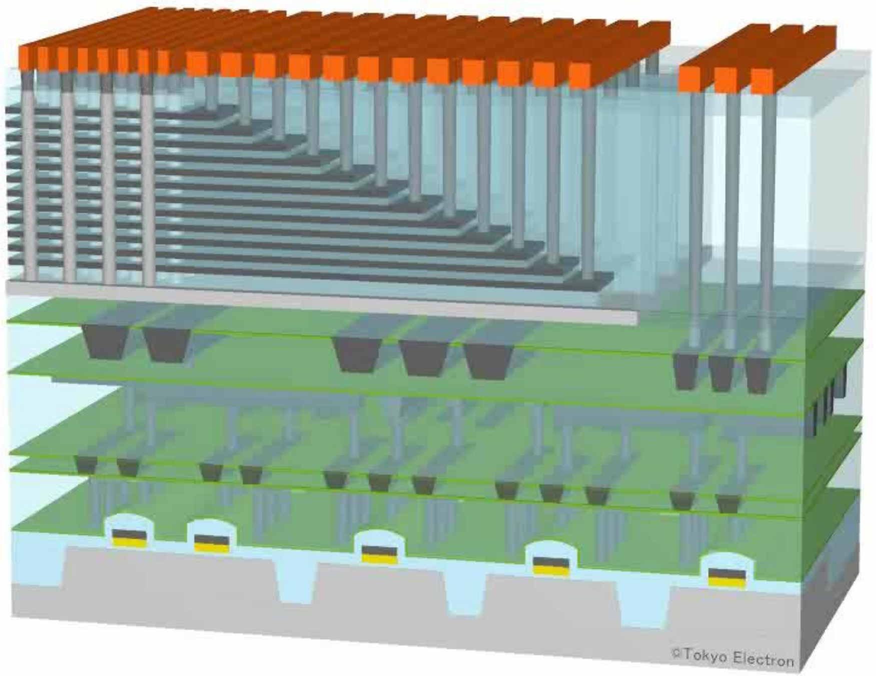
CMOS wafer bonding to enable CbA



Currently evaluating multiple options

NAND Trends and Business Opportunities

Advances in 3D NAND Bit Density



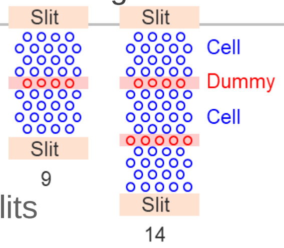
Source: TEL

Reduced device footprint achieved by allocating logic under memory

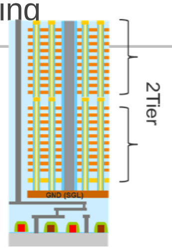
NAND Technology Roadmap

Source: TEL estimates

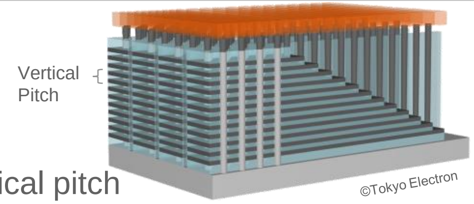
Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Stack (~1.6x/3years)	128L	16x~19xL (176)		22x~25xL (240)	28x~32xL (304)		35x~4xxL (368)	41x~45xL (440)		5xxL (512)	
Tier	1 or 2	2		2	2		2 or 3	3		3 or 4	
Vertical pitch	50~55nm	45~55nm		40~50nm	35~45nm		35~45nm	35~45nm		35~40nm	
Memory height	7~8µm	8.5~10.5µm		10~12.5µm	11~14µm		13.5~17µm	16~20.5µm		18.5~21µm	
Channel		Poly Si grain CIP			incl. MILC Si						
WL metal	W	W		W	Mo		Mo	Mo		Mo	
#of memory holes b/w slits	9	9		9~24	14~24		19 or 24	19 or 24		19 or 24	
Peri. CMOS (In general)	Under array or Next array	Under array		Under array or Bonding	Under array or Bonding		Under array or Bonding	Under array or Bonding		Under array or Bonding	



#of memory holes b/w slits

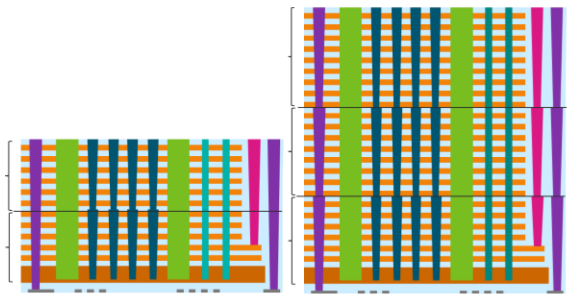
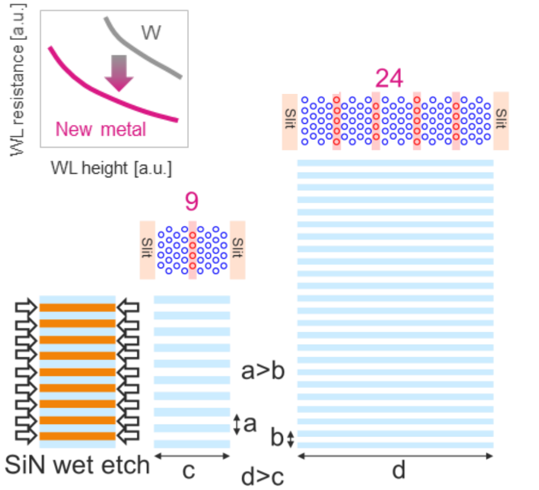
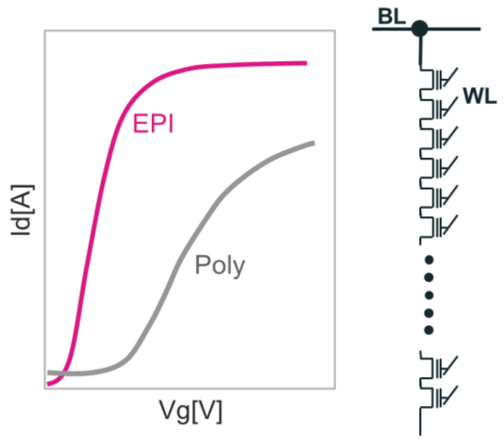
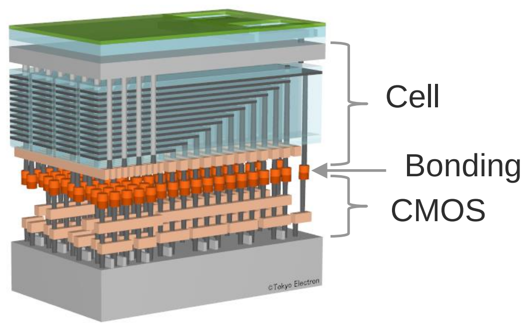


Tier



Vertical pitch

3D NAND Technology Challenges and Solutions

<table>
<tr><th>HARC</th><th>Replacement gate: WL</th><th>Channel Si</th><th>Peri. CMOS bonding</th></tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>・HARC etch: Pluralization of each process (multi-level contact/slit/channel, etc.)</td>
<td>・SiN wet etch: High selective
・Advanced drying: Collapse free
・Mo CVD: Low R WL metal</td>
<td>・CVD Si CIP: Large grain size
→ EPI like</td>
<td>・Cu hybrid bonding</td>
</tr>
</table>

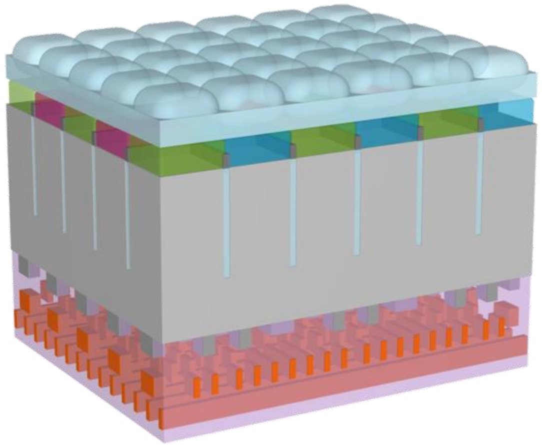
Source: TEL

Processing technology advances essential for enabling further high value-add in NAND devices

CIS Trends and Business Opportunities

CIS Has Expanded Sensor Functions With Onboard AI

Image sensor × **AI** = **Applications**



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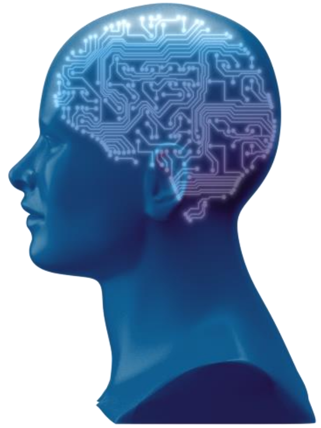

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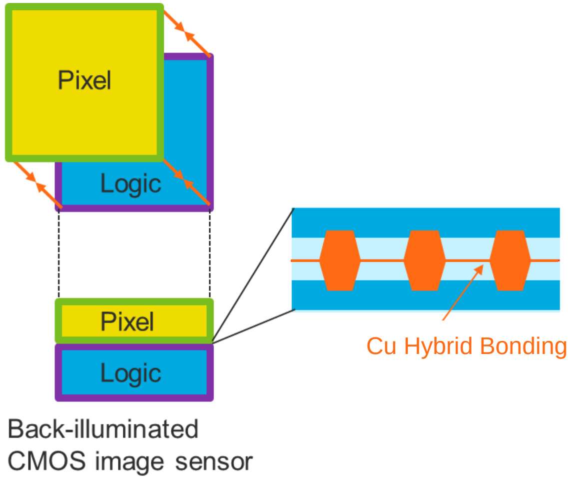
Hybridization of devices is progressing and creating further added-value

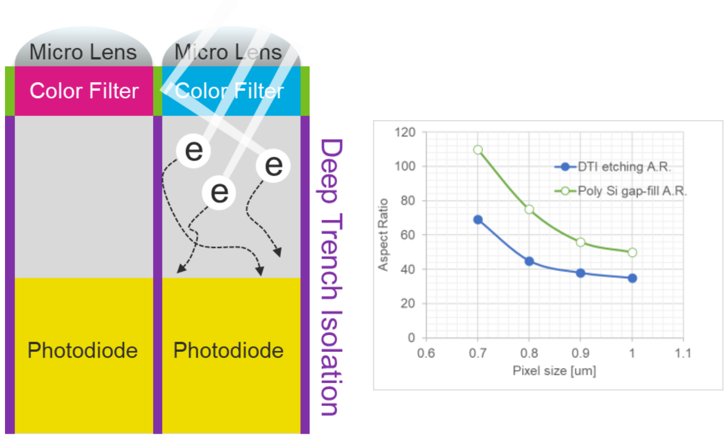
CIS Technology Challenges and Solutions

Wafer bonding: 3D stacked BSI



- Wafer level Cu to Cu hybrid bonding

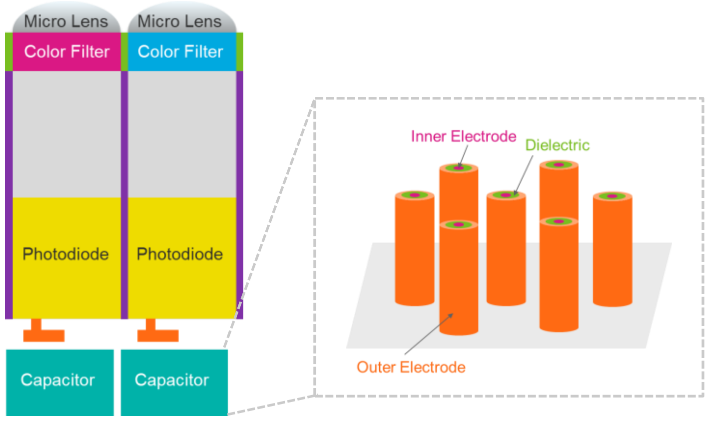
Deep Trench Isolation: Pixel scaling



H. Kim (Samsung) et al. ISSCC 2020 Data edit by TEL

- Si deep trench etch: High A.R. etch
- Poly Si gap-fill: Depo-Etch-Depo for void free fill

Capacitor: Global Shutter



Jae-kyu Lee (Samsung) et al. ISSCC 2020 Schematic by TEL

- Capacitor etch
- Dielectric deposition
- Metal deposition

Increased importance of bonding technology, as well as etch and thin film deposition technology

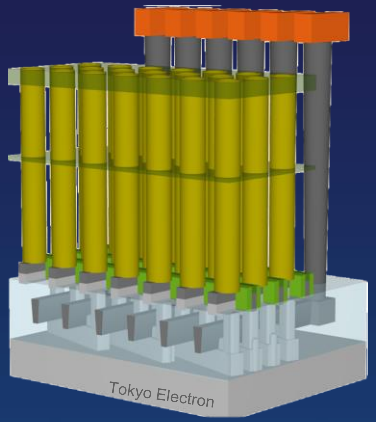
Summary

Summary

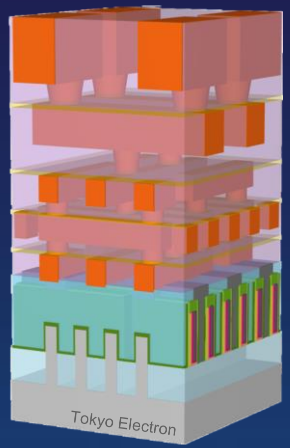
- Market demands are becoming more complex
- To meet these needs, the evolution of devices is accelerating, including multifunctional devices
- Most of the heterogeneity can be covered by existing process and system technologies, but technological evolution is also essential
- Technology development must be undertaken in alignment with environmental issues (SDGs)
- Development of advanced devices leads directly to the SDGs
- TEL's process development is conducted on a worldwide basis, and the company is strongly promoting the development of leading-edge devices through global collaboration both internally and externally
- And what else?

Metaverse

Working memory



AI & Data processing



Storage memory

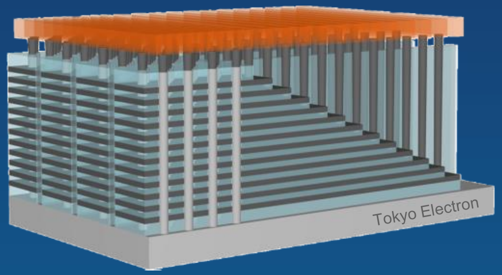
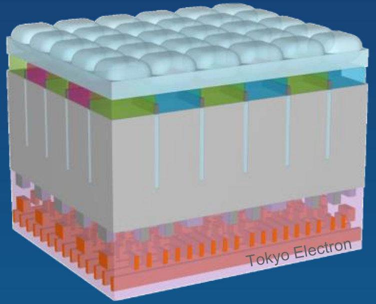


Image sensing



Semiconductor devices enable Metaverse

TEL

Smart Portable Devices are Loaded with High End Devices

Smart Phone is still one of the platforms that drives technology

TEL

Internet of Automobiles

Massive sensor data generators especially from autonomous driving autos

TEL

Internet of People

People are becoming sensor-ized data generators

TEL

Metaverse

Semiconductor devices enable Metaverse

TEL

TEL

TOKYO ELECTRON

SPE Business Strategy

July 12, 2022

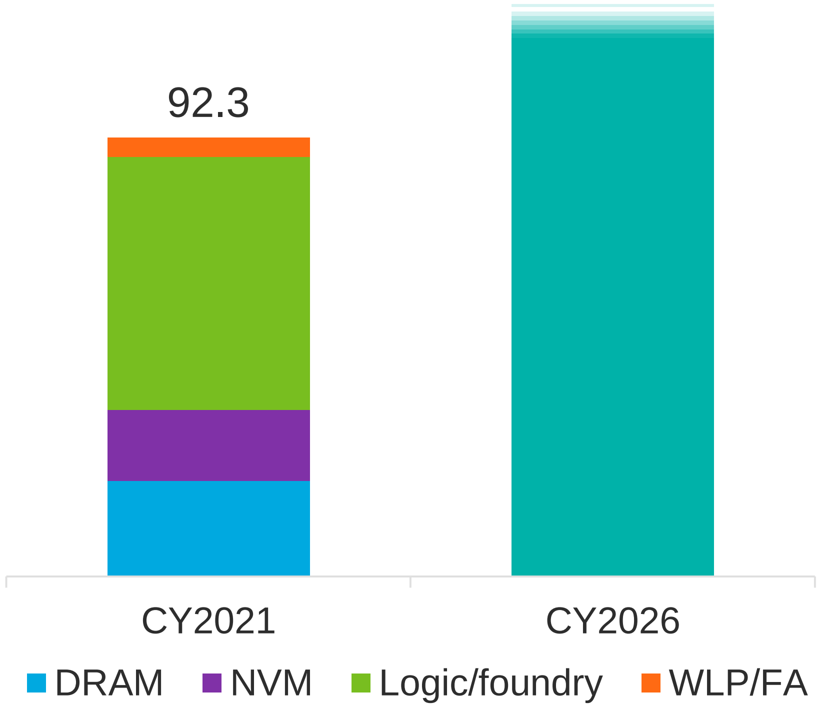
Yoshinobu Mitano
Corporate Officer, Executive Vice President and General Manager
SPE Business Division

Overview

- WFE Market and Technological Requirements by Application
- SPE Segment Sales Target and Business Opportunities
- Development Efforts
  - Strengthen R&D Capabilities
  - Increase in New Product Sales Composition Ratio
  - Increase Environmental Performance
  - Increase Efficiency of Equipment Start-up
- Hot Topics
  - EUV Patterning Technology
  - Backend Business Strategy
- Summary

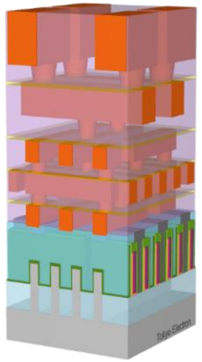
WFE Market and Technological Requirements by Application

WFE Market Growth (USB$)

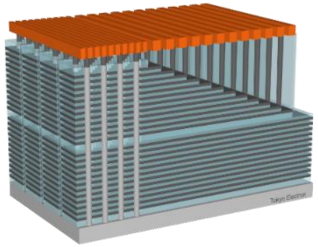


Technological Requirements

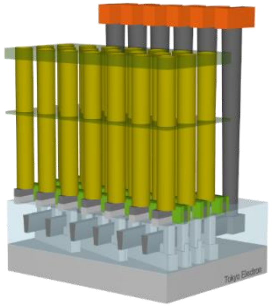
- Logic/foundry：
  - Scaling along with structural changes
    - ➢ Reduction in manufacturing cost per transistor
    - ➢ Lowering power consumption
    - ➢ Higher performance



- NAND
  - Increasing the layer counts
    - ➢ Reduction in manufacturing cost per bit

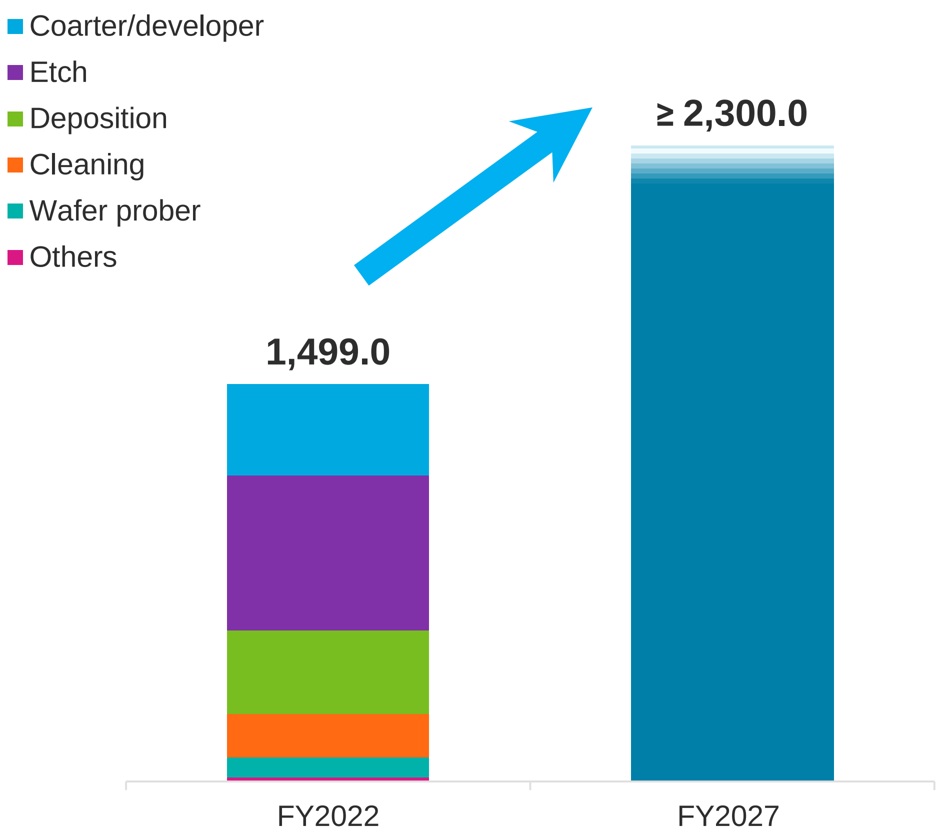


- DRAM
  - Scaling to realize
    - ➢ Reduction in manufacturing cost per bit
    - ➢ Lowering power consumption
    - ➢ Higher performance



SPE Segment Sales Target and Business Opportunities

SPE New Equipment Sales Target ($B)

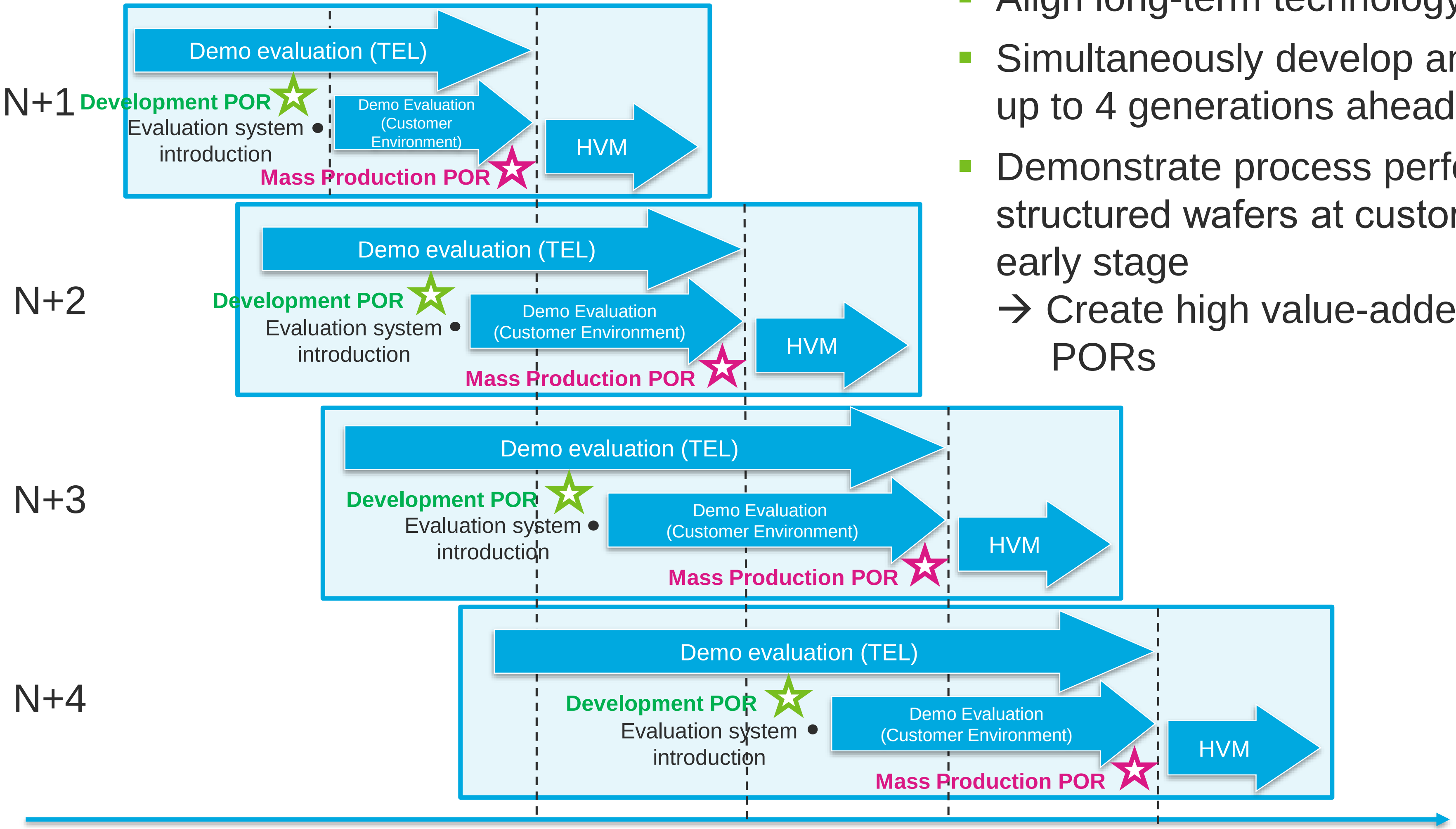


Business Opportunities

- Logic/foundry
  - Increase patterning complexity requires co-optimization between unit processes
  - Adoption of High-NA EUV lithography
  - Adoption of GAA and backside PDN
- NAND
  - 3D NAND layer counts reach more than 300 layers
  - High aspect ratio etch, high productivity sacrificial film removal and atomic-level deposition on 3D structure
- DRAM
  - Technology to suppress RC delay in wiring
  - Capacitor formation technology for further scaling

Development Efforts

Simultaneous 4-Generation Developments



- Align long-term technology roadmap with customers
- Simultaneously develop and evaluate technologies up to 4 generations ahead
- Demonstrate process performance on customer structured wafers at customer's environments at early stage
  → Create high value-added products and acquire PORs

Strengthen R&D Capabilities

Yamanashi R&D building

Deposition system, gas chemical etch system, corporate R&D
(Completion scheduled for spring 2023)

Kumamoto R&D building

Coater/Developers, surface preparation system
(Completion scheduled for fall 2024)

Miyagi R&D building

Etch system
(Completion scheduled for spring 2025)

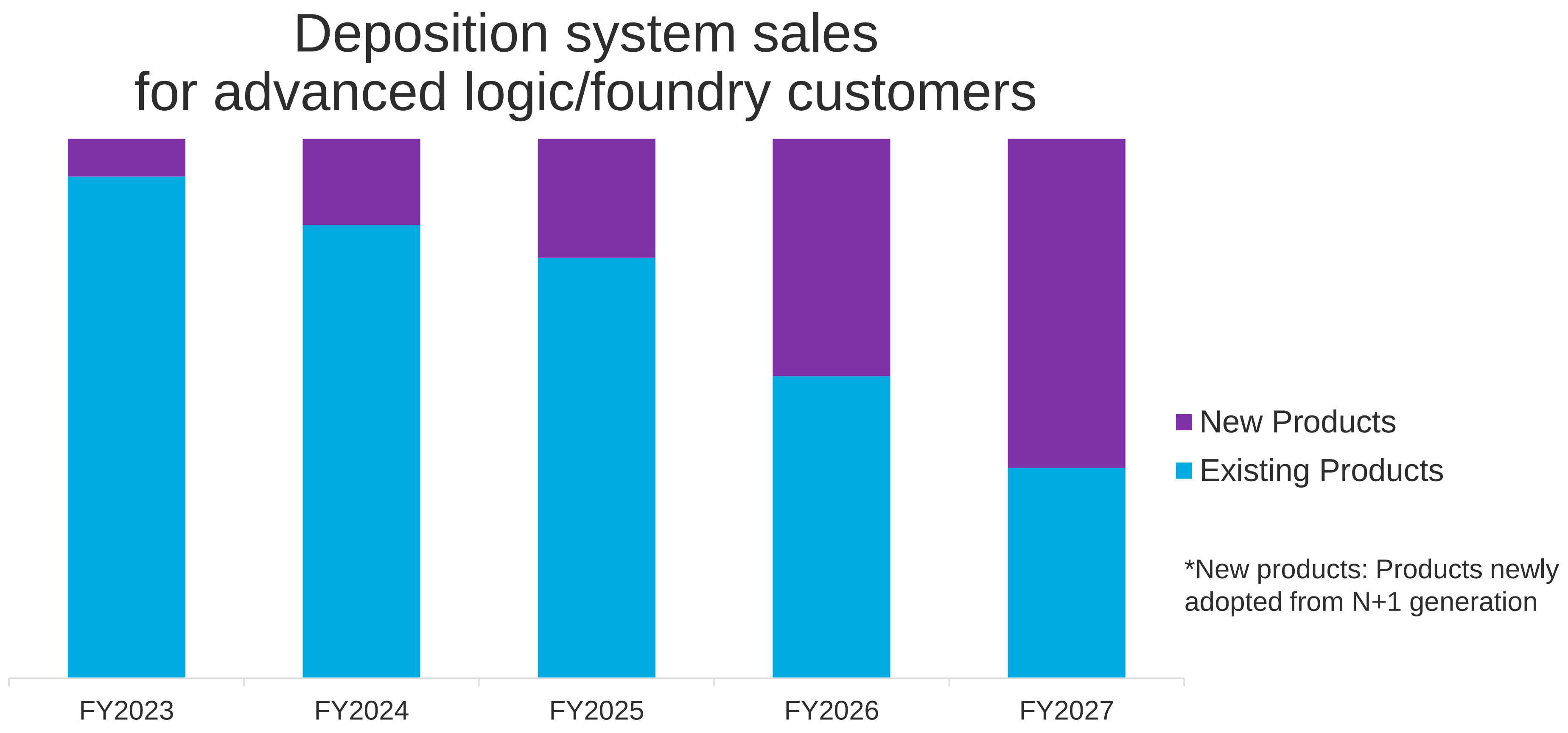
Miyagi Technology Innovation Center

Etch system
(Began operation in Oct. 2021)

TEL Digital Design Square

DX, Software
(Began operation in Nov. 2020)

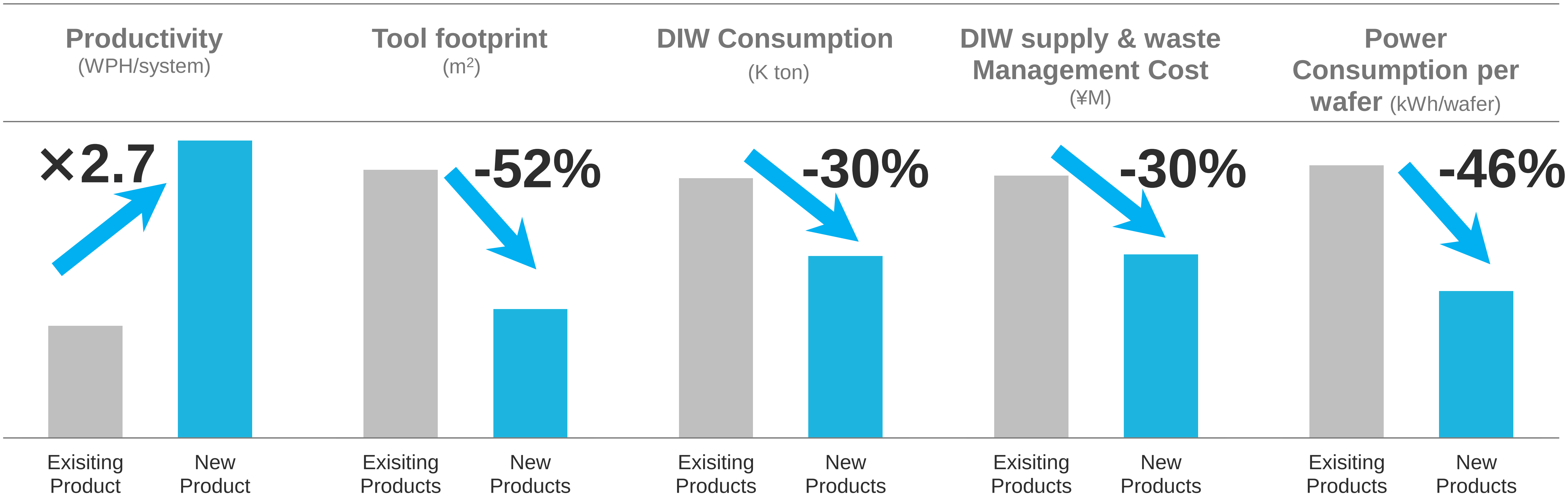
Increase in New Product Sales Composition Ratio



The proportion of high value-added products will increase.
Contribute to enhancing sales, profits and market share

Increase Environmental Performance

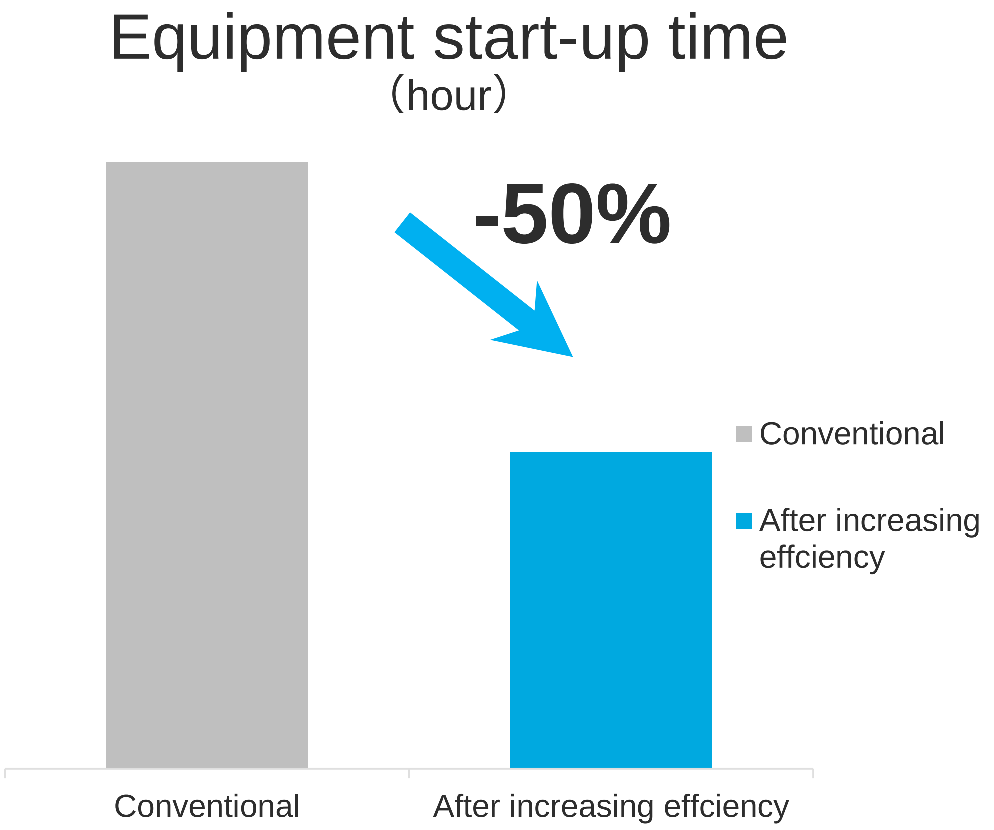
Cleaning system



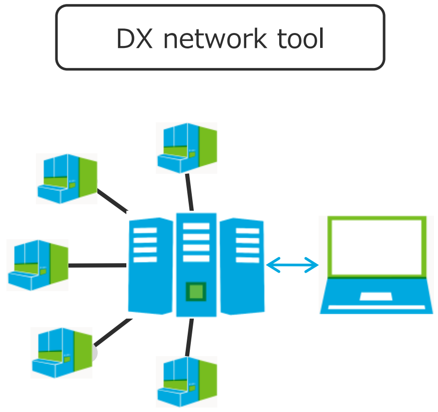
Environmental performance = equipment performance

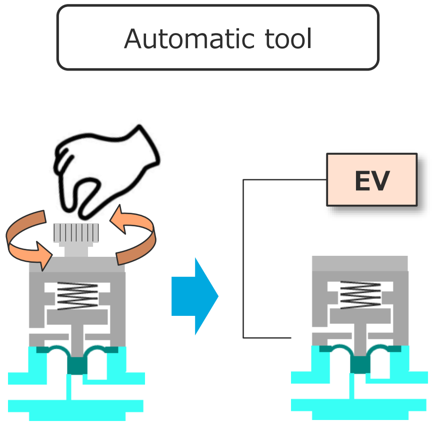
Further enhance environmental performance

Increase Efficiency of Equipment Start-up



- Measures：
  - Optimize inspection items and automate inspection
  - Expand online support
  - DX network tool
  - Automatic tool





Further enhance customer satisfaction and productivity

Hot Topic 1 : EUV Patterning Technology

CLEAN TRACK™ LITHIUS Pro™ Z EUV : Coater/Developer

LITHIUS Pro Z released in 2012 (Total shipment **> 2000 systems**) → Releasing new EUV CAR/MOR compatible features

LITHIUS Pro Z EUV
Total shipment > 140 systems

High Reliability
100% market share in in-line coater/developer for EUV

High Productivity
Maximize EUV exposure tool performance

High Versatility
Applicable to Metal Oxide Resists and underlayers in addition to Chemically Amplified Resists

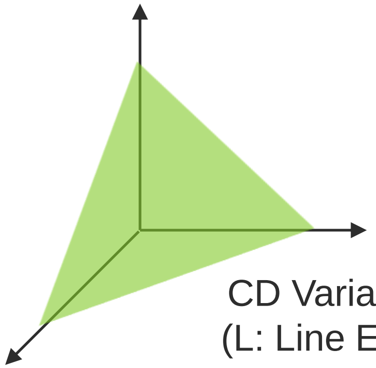
The LITHIUS Pro Z platform, which has a long track record of mass production for exposure tools with a variety of light sources, has the above three strengths

EUV Lithography Process: Roadmap and Challenges

Line pitch (nm)	34	32	30	28	26	24	22	20
Hole/pillar pitch (nm)	42	40	38	36	34	32	30	28
Roadmap of EUV exposure equipment and resist technology	0.33 NA EUV (Single exposure or multi-patterning) 0.55 NA (High NA) EUV (Single exposure or multi-patterning) Chemically Amplified Resist (CAR) Metal Oxide Resist (MOR)							

RLS trade off

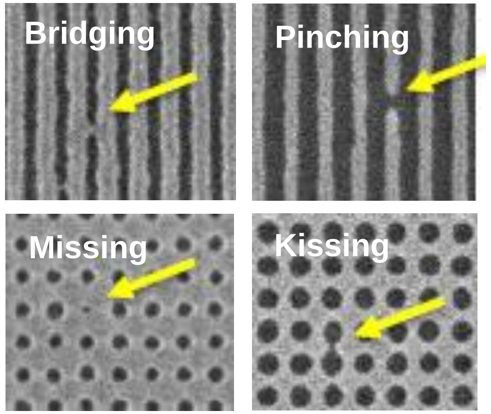
Sensitivity (S)



Resolution (R)

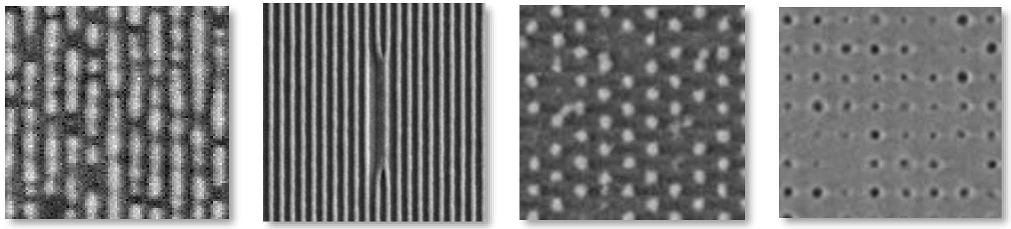
CD Variation (L: Line Edge Roughness)

Defects induced by variation in EUV lithography



P. De Bisschop, Proc. SPIE, 10957-10 (2019)

Issues of securing required resist film thickness



Post-etch resist damage

Resist line collapse

Resist pillar collapse

Residue inside hole

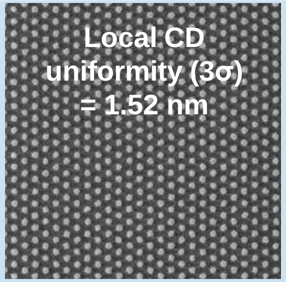
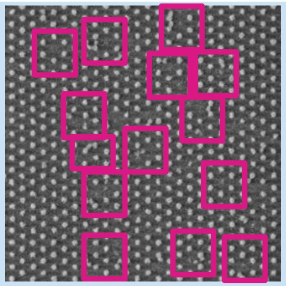
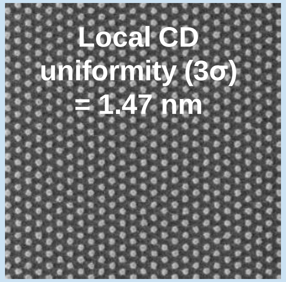
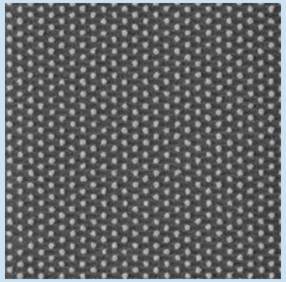
Challenges for Thinning Resist Film

Challenges for Thickening Resist Film

TEL is providing patterning solutions for the EUV challenges

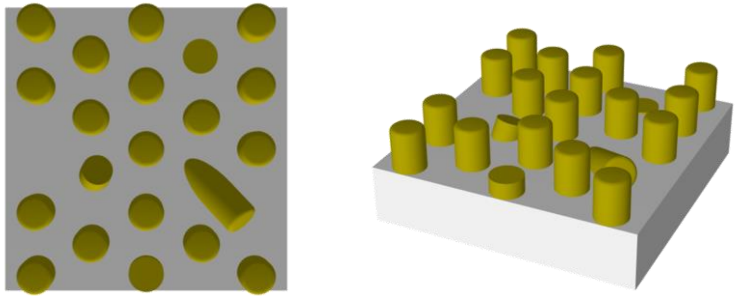
New Development Method: ESPERT*™ for Pillar Metal Oxide Resist

36 nm pitch 18 nm pillar for DRAM (after lithography)

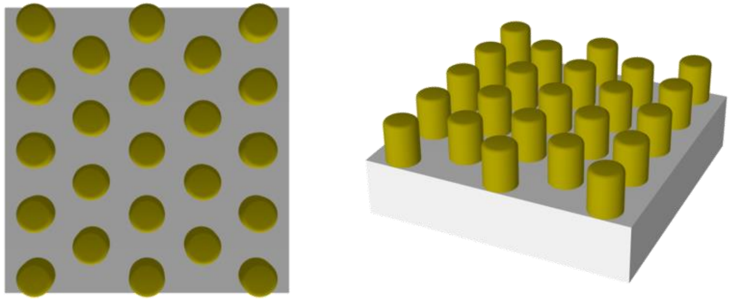
Conventional wet development technology		
	CD 18.0 nm EUV exposure 99.5 mJ/cm^2	15.1 nm 86.0 mJ/cm^2
Newly developed development technology; ESPERT		
	CD 18.0 nm EUV exposure 75.5 mJ/cm^2	15.2 nm 66.5 mJ/cm^2

Source: TEL, Resist film thickness: 22 nm

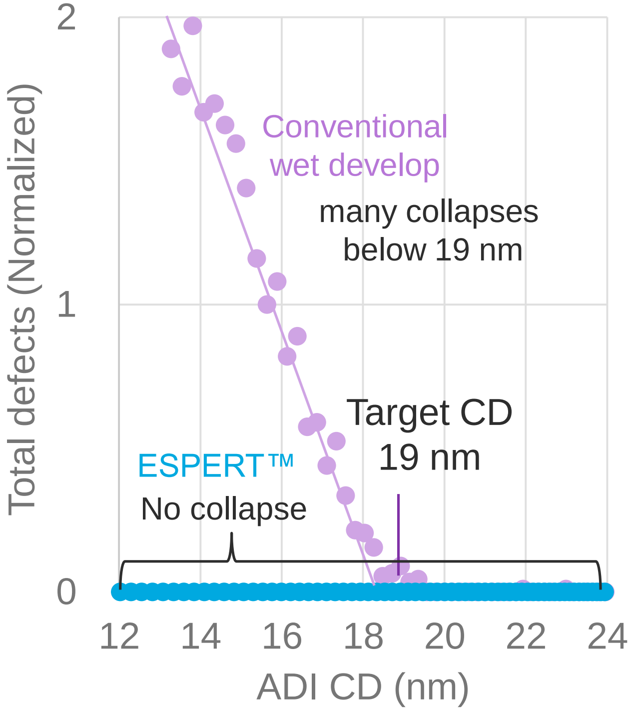
Resist collapse with conventional development technology



New wet development technology prevents resist collapse



Enhanced pillar pattern collapse margin



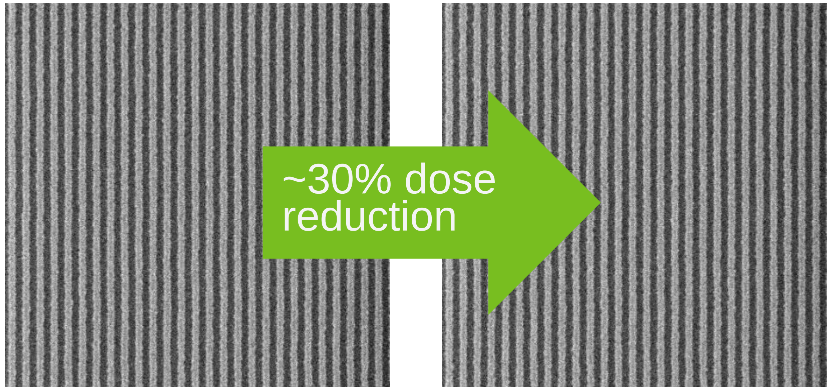
ESPERT prevents resist collapse, reduces EUV exposure dose by 25% and decreases CD variations

*Enhanced Sensitivity Developer Technology

New Development Method: ESPERT for L/S Metal Oxide Resist

Roughness and profile @ 30 nm-pitch (after development)

REFERENCE | ESPERT

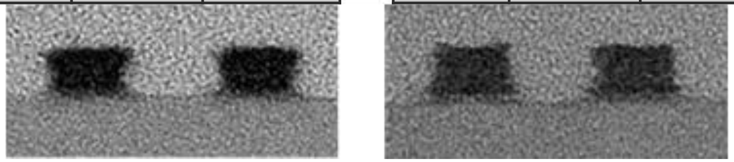


REFERENCE:

DCD (nm)	Unb. LER (nm)	Unb. LWR (nm)
14.3	2.2	3.0

ESPERT:

DCD (nm)	Unb. LER (nm)	Unb. LWR (nm)
14.5	2.2	2.9

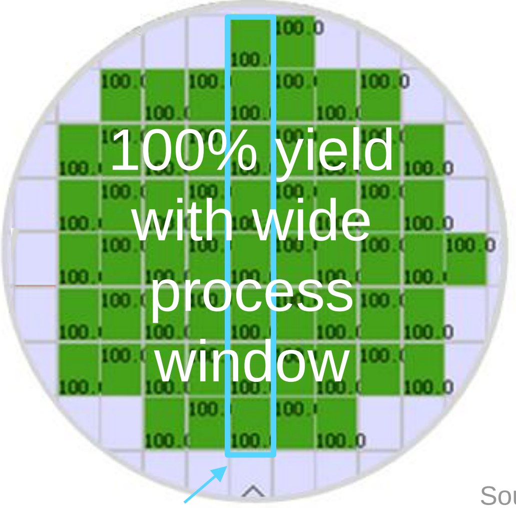


Source: TEL

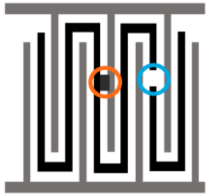
ESPERT can tune resist profile

Opens and shorts test @ 30 nm-pitch

ESPERT



Open-short test patterns



Source: TEL/IBM SPIE2022

EUV dose change

Dose stripe e-test performance (CD 13.2 nm ~ 15.6 nm)

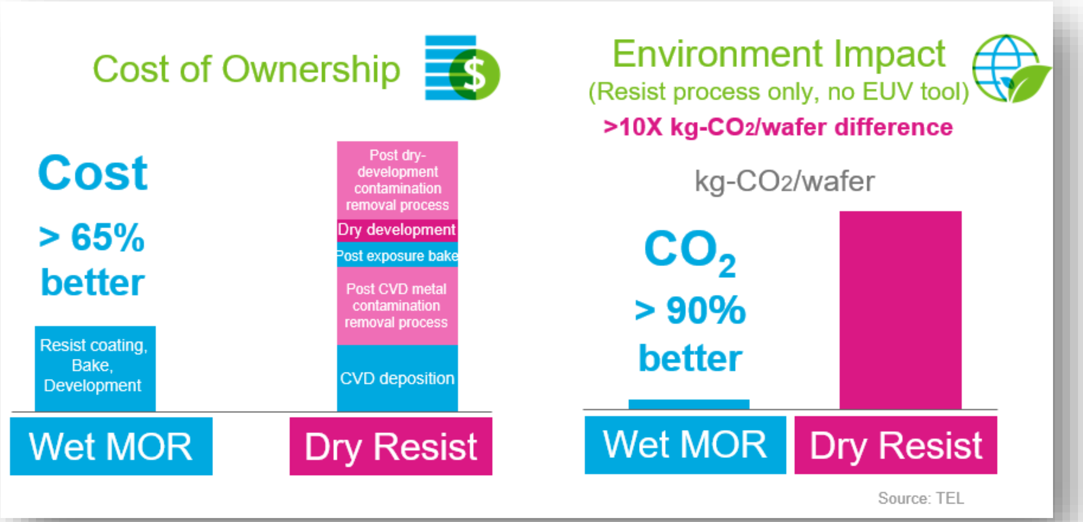
ESPERT on 30 nm pitch L/S shows ~30% dose reduction without roughness penalty. 100% yield data with wide process window were confirmed

Benchmarking Wet MOR and Dry Resist in EUV Lithography

Wet MOR
TEL/inpria

#1 (All-in-One)

COT → EUV → PEB DEV



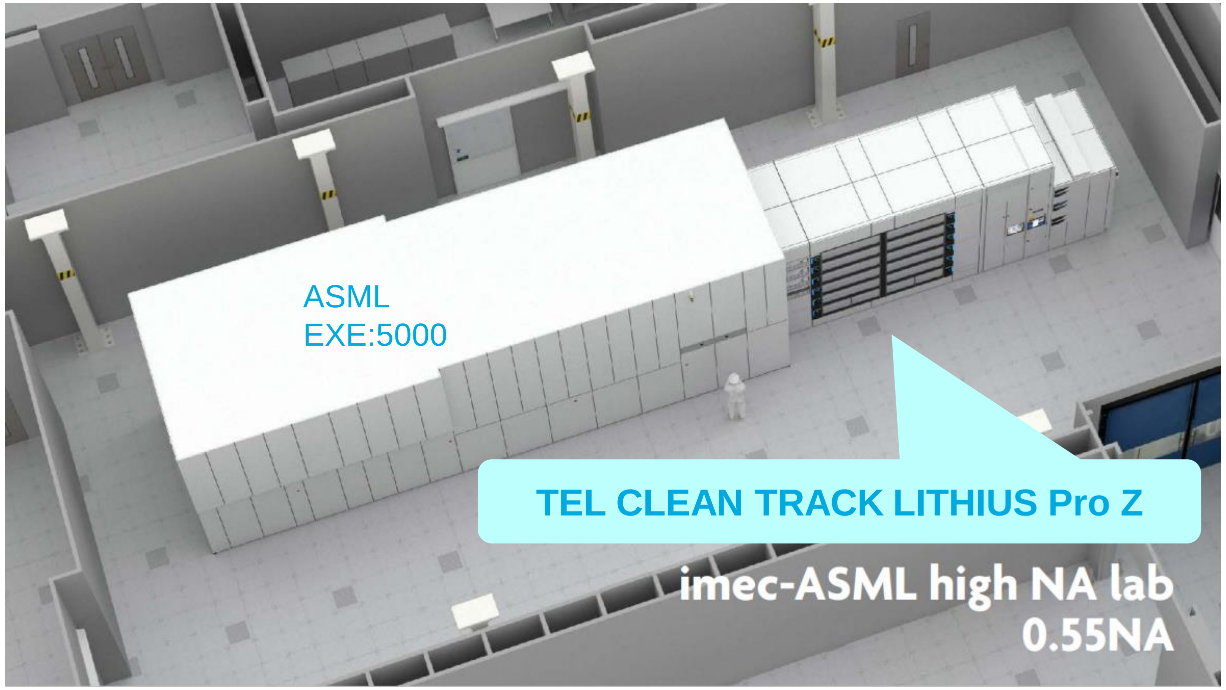
Dry Resist
TEL's estimate

#1	#2	#3	#4	#5	#6
CVD PAB	CLEAN	EUV	PEB	2nd PEB/ DRY DEV	CLEAN

Dry Resist:
- Longer TAT/Q-time
- Larger footprint (> 5x?)
- Limitation for resist type

TEL's MOR process provides higher economic/environmental values than Dry Resist

TEL LITHIUS Pro Z for imec-ASML High NA EUV Joint Lab



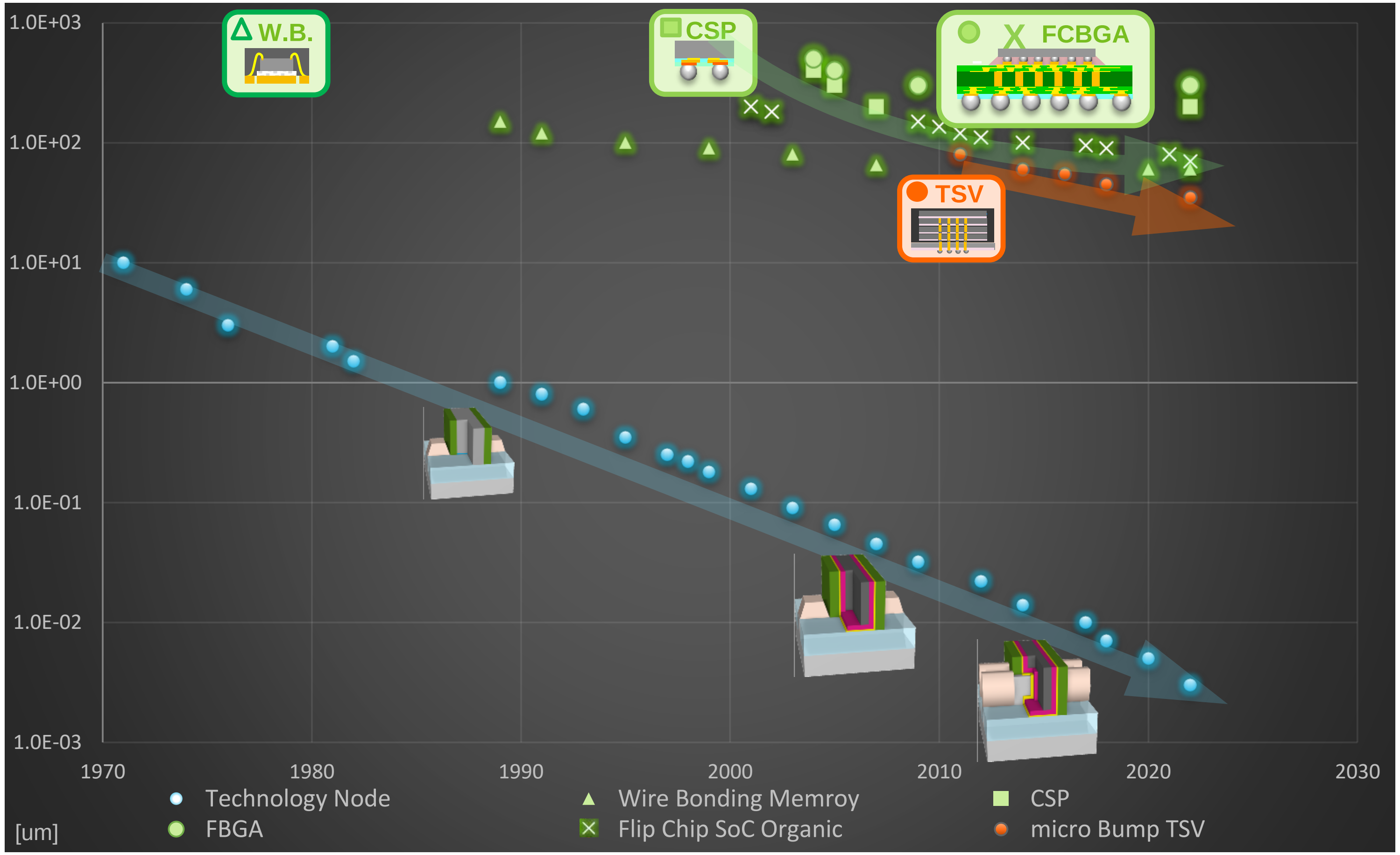
Courtesy of imec

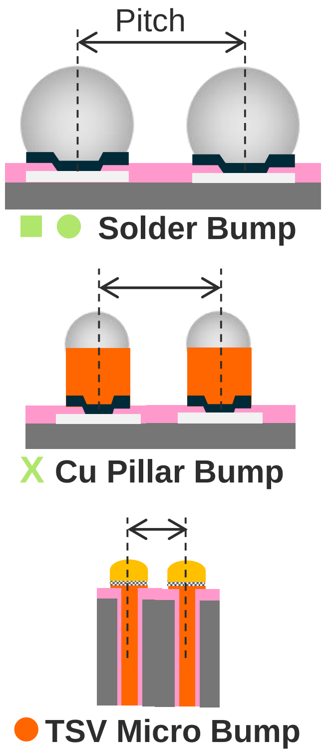
High NA EUV for higher resolution

- TEL has shipped advanced modules on **TEL CLEAN TRACK LITHIUS Pro Z** for the high NA exposure tool
- First prototype high NA EUV exposure tool is available in 2023 at the High NA lab
- A three-year program is planned for the Pre HVM validation

Hot Topic 2 : Backend Business Strategy

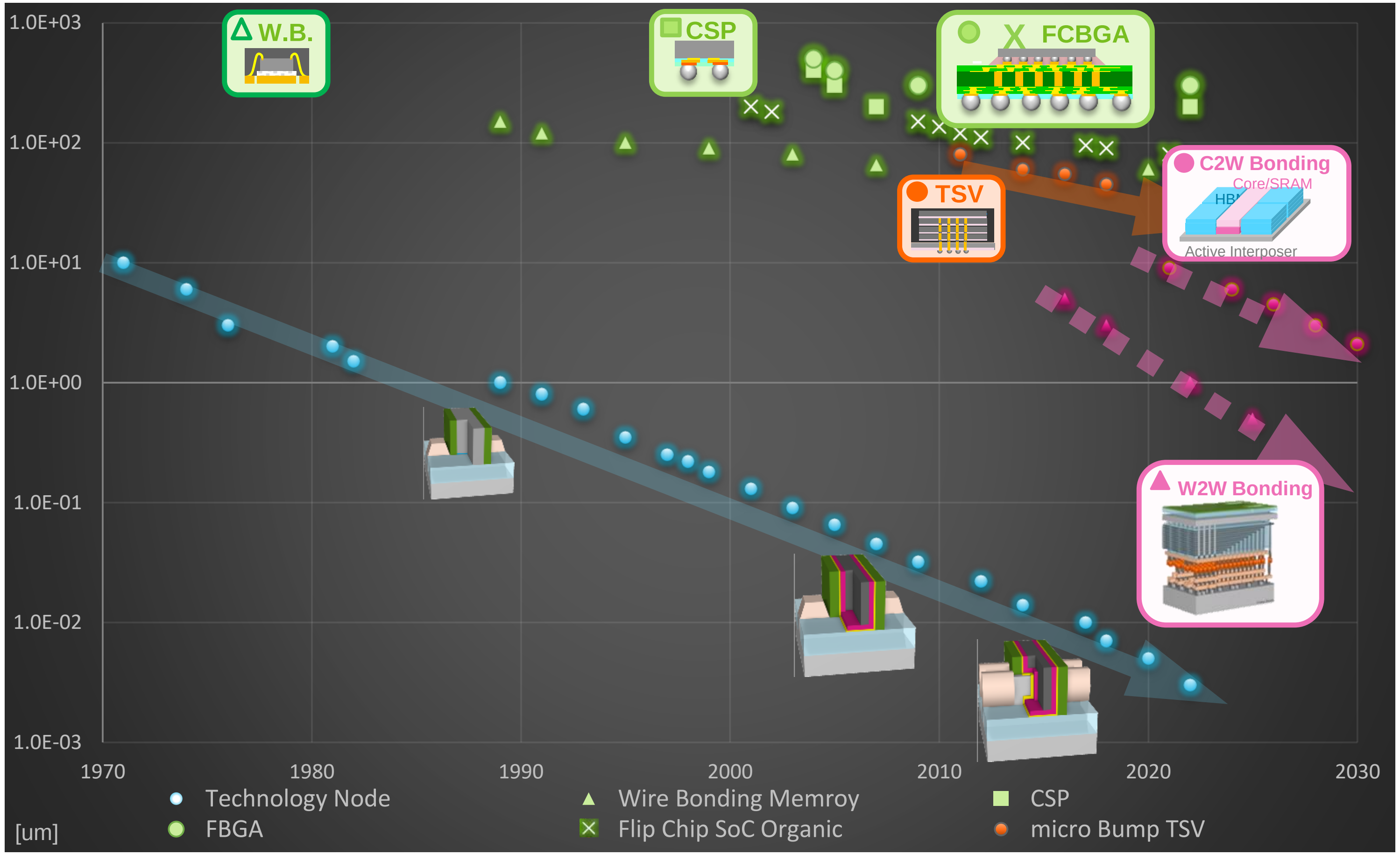
Semiconductor Technology Node and Bump Pitch

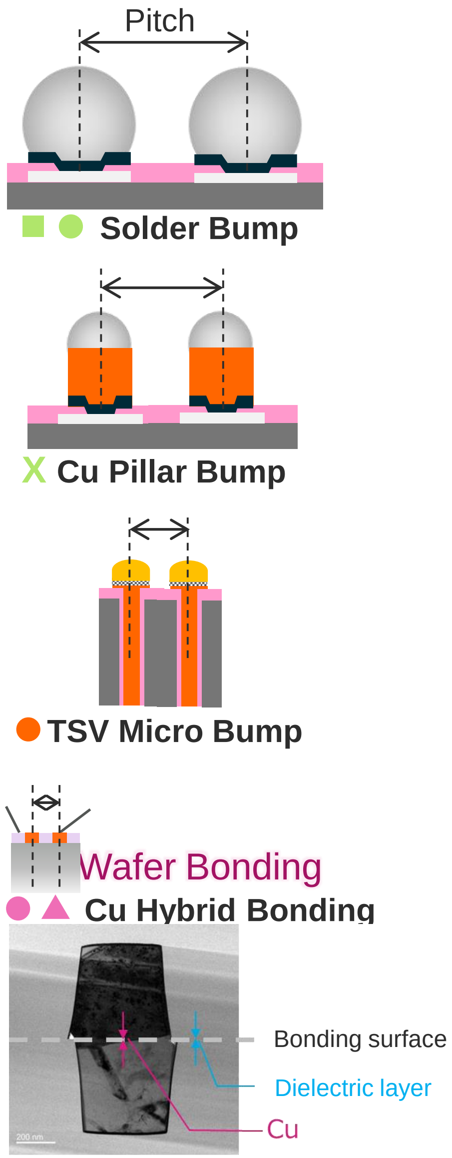




Introduction of wafer bonding technology accelerates further reduction of pitch

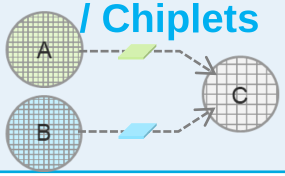
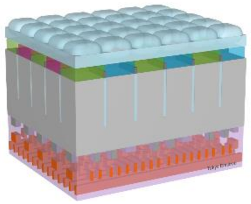
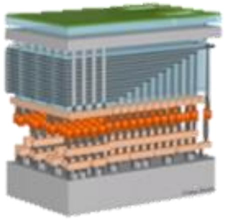
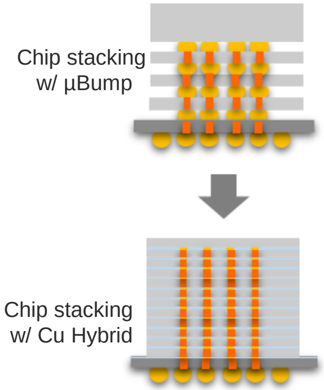
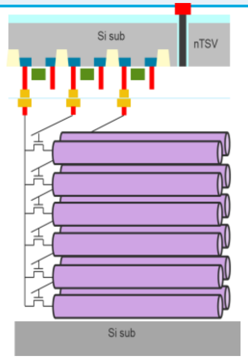
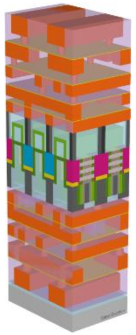
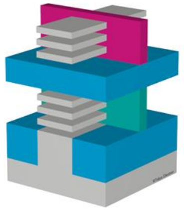
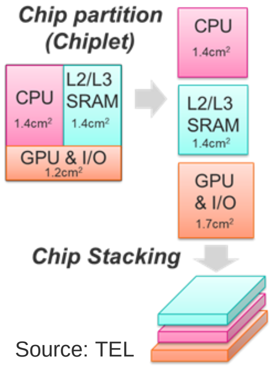
Semiconductor Technology Node and Bump Pitch





Introduction of wafer bonding technology accelerates further reduction of pitch

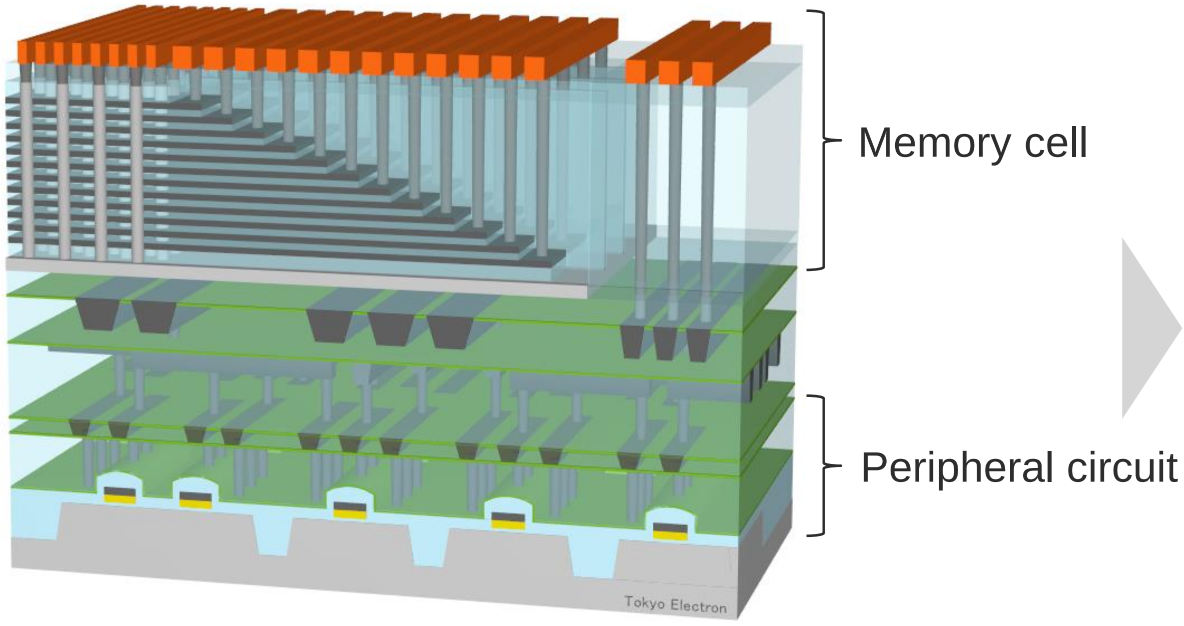
Application of Wafer Bonding

Device	CIS	NAND	DRAM		Logic		
Stacking Device	**BSI** Sensor + (Memory) + Logic	**3D NAND** Cell + Peripheral	**HBM** DRAM ⋮ DRAM + Logic	**3D DRAM** Cell + Peripheral	**Backside PDN** Logic + Bare Si	**Sequential CFET** Logic + Logic	**Disaggregation / Chiplets** 
Bonding	W-W Cu Hybrid	W-W Cu Hybrid	D-W Cu Hybrid	W-W Cu Hybrid	W-W Ox Fusion	W-W Ox Fusion	D-W / D-D Cu Hybrid
3D I/O Pitch	3 µm →1 µm	1 µm →0.5 µm	40 µm →25 µm	1 µm →0.5 µm	Sub µm (nTSV)	Sub µm (nTSV)	10 µm →1 µm
Structure				 Source: TEL 3D DRAM structure			 Source: TEL
Status	HVM	R&D~HVM	R&D	R&D	R&D	R&D	R&D

Expanding adoption of wafer bonding technology for next-generation devices

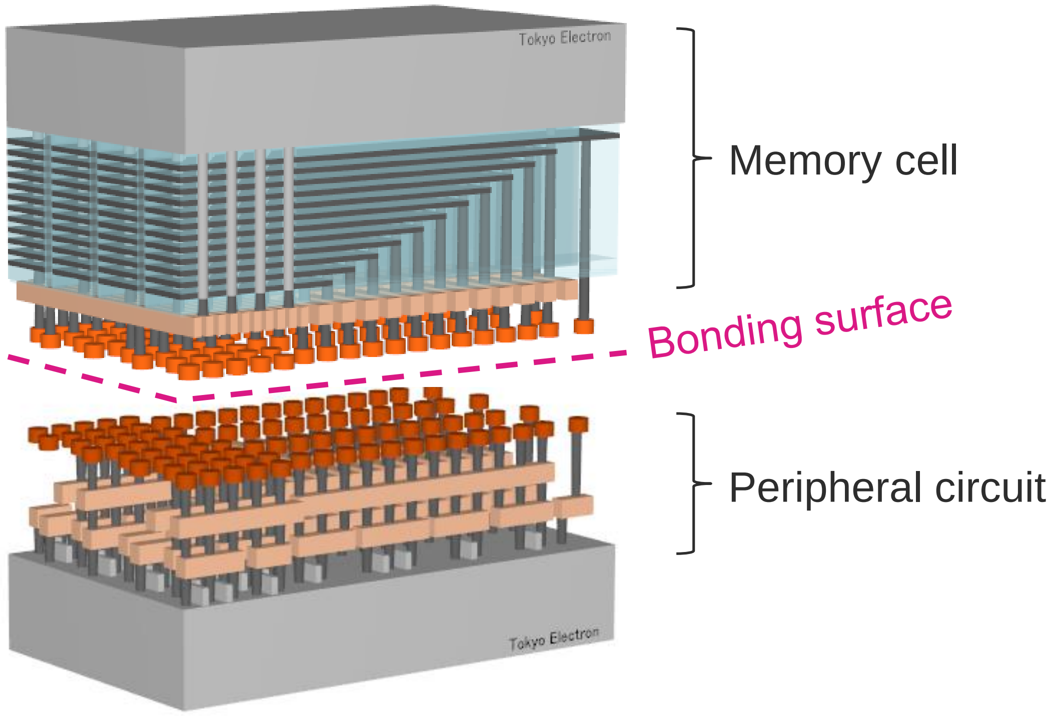
Wafer Bonding Application for 3D NAND

Current structure



- ✓ Peripheral circuit performance deteriorates due to exposure to high temperature during memory cell manufacturing
- ✓ Long interconnects wiring

New structure

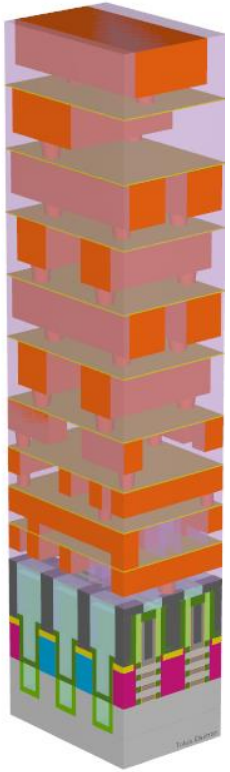


- ✓ Peripheral circuit is manufactured on the separate wafer and bond to the memory cell wafer
  - higher peripheral circuit performance
  - shorter TAT* process
- ✓ Shorter interconnects wiring

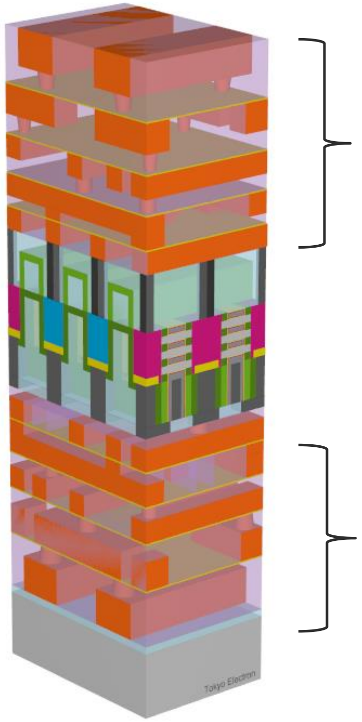
* TAT: Turnaround time

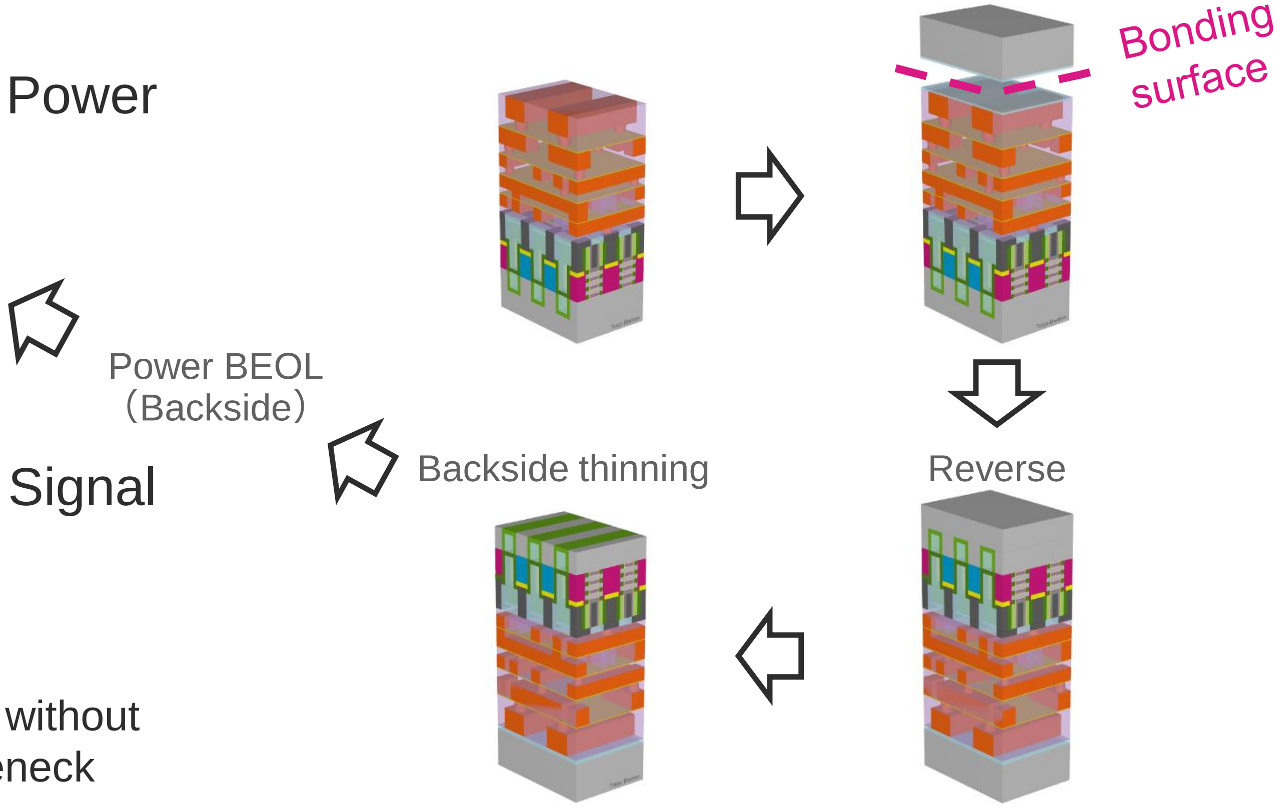
Wafer Bonding Application for Logic Backside PDN

Current structure



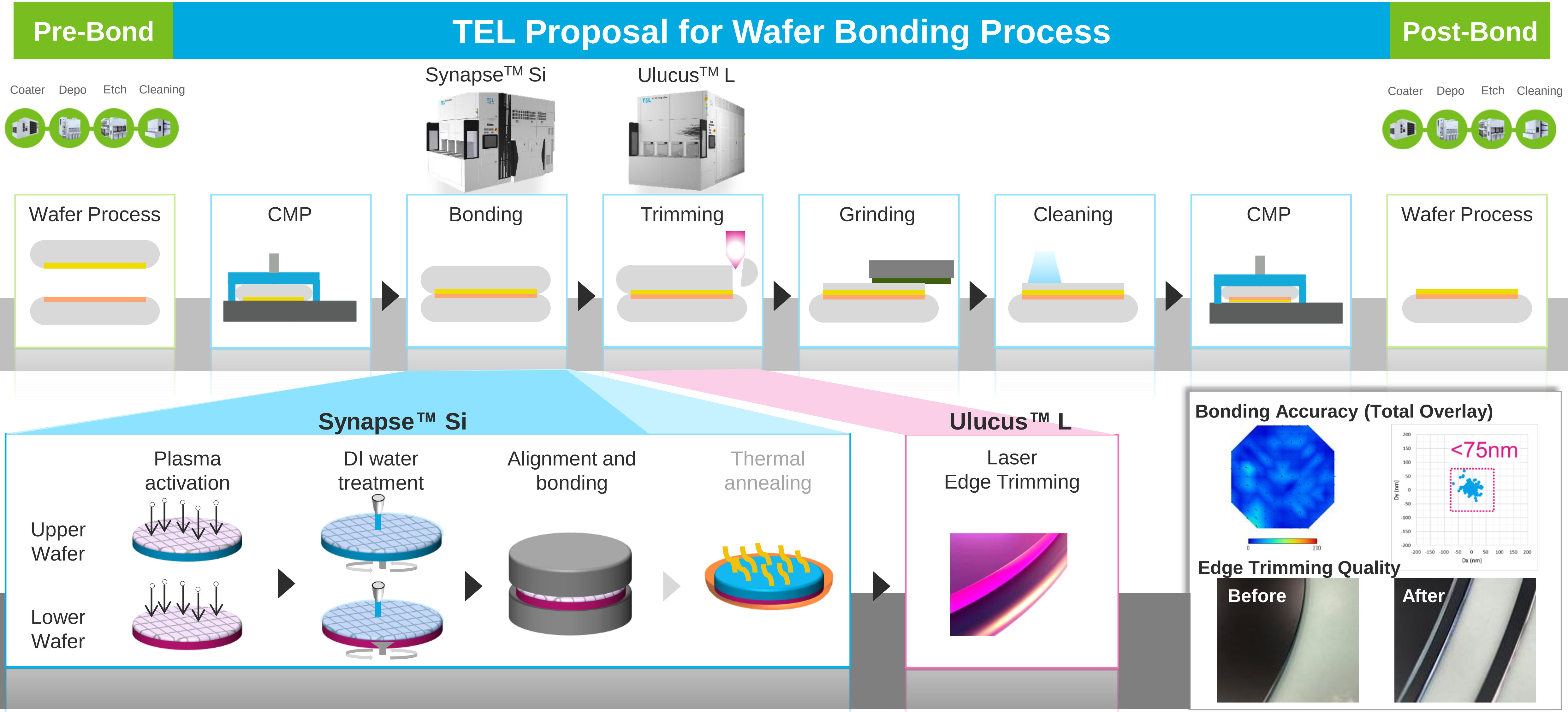
Backside PDN : Power Delivery Network





Pursue further scaling without
the power wiring bottleneck

Our Proposal for Wafer Bonding Process



Summary

- Business opportunities are expanding along with the technological innovation in both logic and memory
- Provide added value through co-optimization of our wide range of products
- Create high value-added equipment and acquire PORs through 4-generation simultaneous developments and evaluations with our customers
- Enhance and strengthen development capabilities
- Enhance customer satisfaction and productivity by shortening equipment start-up times using DX and AI

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